L Number	Hits	Search Text	DB	Time stamp
1	2532	(rout$4 same (pitch or spac$3)) same layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:23
2	662	((rout$4 same (pitch or spac$3)) same layer) and vertical and horizontal and connect$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:27
3	40	(pitch same vertical) and (pitch same horizontal) and ((rout$4 same (pitch or spac$3)) same layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:28
4	26	((pitch same vertical) and (pitch same horizontal) and ((rout$4 same (pitch or spac$3)) same layer)) and connect$5 and configur$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:32
5	6	(((pitch same vertical) and (pitch same horizontal) and ((rout$4 same (pitch or spac$3)) same layer)) and connect$5 and configur$5) and (PLD or (programmable adj logic adj device))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:43
6	3	(((pitch same vertical) and (pitch same horizontal) and ((rout$4 same (pitch or spac$3)) same layer)) and connect$5 and configur$5) and embed$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:44
7	19	(((pitch same vertical) and (pitch same horizontal) and ((rout$4 same (pitch or spac$3)) same layer)) and connect$5 and configur$5) and direction	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:44
-	47446	rout$4 and (pitch or spac$3) and vertical and horizontal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:08
-	15333	(rout$4 and (pitch or spac$3) and vertical and horizontal) and layer and connect$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:25
-	9034	(rout$4 same (pitch or spac$3)) and vertical and horizontal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:23
-	3330	((rout$4 same (pitch or spac$3)) and vertical and horizontal) and layer and connect$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:07
-	2550	(((rout$4 same (pitch or spac$3)) and vertical and horizontal) and layer and connect$5) and configur$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:32
-	2943	rout$4 same (pitch or spac$3) same (vertical or horizontal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:08

-	2550	((((rout$4 same (pitch or spac$3)) and vertical and horizontal) and layer and connect$5) and configur$5) and configur$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:09
-	1642	(rout$4 same (pitch or spac$3) same (vertical or horizontal)) and configur$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:10
-	682	((rout$4 same (pitch or spac$3) same (vertical or horizontal)) and configur$5) and layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:10
-	111	(((rout$4 same (pitch or spac$3) same (vertical or horizontal)) and configur$5) and layer) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:17
-	9736	(pitch same vertical) and (pitch same horizontal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 06:28

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030234583 A1	20031225	16	Repeater methods for constrained pitch wire buses on integrated circuits	307/147
2	US 20030229837 A1	20031211	15	Method and apparatus for testing a logic cell in a semiconductor device	714/737
3	US 20030206145 A1	20031106	15	Scanned display systems using color laser light sources	345/84
4	US 20030080777 A1	20030501	31	Programmable logic device structures in standard cell devices	326/39
5	US 20030049886 A1	20030313	30	Electronic system modules and method of fabrication	438/106
6	US 20030025205 A1	20030206	56	Hexadecagonal routing	257/758
7	US 20020186045 A1	20021212	15	Cell architecture to reduce customization in a semiconductor device	326/41
8	US 20020048849 A1	20020425	16	Stackable flex circuit IC package and method of making same	438/109
9	US 20010049813 A1	20011206	19	INTEGRATED CIRCUIT INCORPORATING A POWER MESH	716/8
10	US 6675309 B1	20040106	30	Method for controlling timing in reduced programmable logic devices	713/401
11	US 6629308 B1	20030930	31	Method for managing database models for reduced programmable logic device components	716/16
12	US 6611951 B1	20030826	21	Method for estimating cell porosity of hardmacs	716/12
13	US 6590289 B2	20030708	34	Hexadecagonal routing	257/758
14	US 6580289 B2	20030617	14	Cell architecture to reduce customization in a semiconductor device	326/40
15	US 6532572 B1	20030311	11	Method for estimating porosity of hardmacs	716/4

	Document ID	Issue Date	Pages	Title	Current OR
16	US 6526563 B1	20030225	31	Method for improving area in reduced programmable logic devices	716/18
17	US 6526555 B1	20030225	60	Method for layout and manufacture of gridless non-manhattan semiconductor integrated circuits using compaction	716/11
18	US 6522336 B1	20030218	38	Three-dimensional graphics rendering apparatus and method	345/582
19	US 6515509 B1	20030204	30	Programmable logic device structures in standard cell devices	326/39
20	US 6514793 B2	20030204	14	Stackable flex circuit IC package and method of making same	438/109
21	US 6490707 B1	20021203	31	Method for converting programmable logic devices into standard cell devices	716/2
22	US 6480989 B2	20021112	17	Integrated circuit design incorporating a power mesh	716/8
23	US 6426549 B1	20020730	16	Stackable flex circuit IC package and method of making same	257/686

	Document ID	Issue Date	Pages	Title	Current OR
24	US 6323060 B1	20011127	14	Stackable flex circuit IC package and method of making same	438/109
25	US 6198635 B1	20010306	16	Interconnect layout pattern for integrated circuit packages and the like	361/760
26	US 5990502 A	19991123	11	High density gate array cell architecture with metallization routing tracks having a variable pitch	257/202
27	US 5977574 A	19991102	11	High density gate array cell architecture with sharing of well taps between cells	257/207
28	US 5929469 A	19990727	27	Contact holes of a different pitch in an application specific integrated circuit	257/208
29	US 5923059 A	19990713	17	Integrated circuit cell architecture and routing scheme	257/204
30	US 5912464 A	19990615	21	Infrared detector and manufacturing process	250/338.4

	Document ID	Issue Date	Pages	Title	Current OR
31	US 5898194 A	19990427	15	Integrated circuit cell architecture and routing scheme	257/206
32	US 5723883 A	19980303	18	Gate array cell architecture and routing scheme	257/204
33	US 5317344 A	19940531	17	Light emitting diode printhead having improved signal distribution apparatus	347/237
34	US 5311443 A	19940510	8	Rule based floorplanner	716/10
35	US 5295082 A	19940315	27	Efficient method for multichip module interconnect	716/12
36	US 5255156 A	19931019	24	Bonding pad interconnection on a multiple chip module having minimum channel width	361/783
37	US 5224022 A	19930629	11	Reroute strategy for high density substrates	361/777
38	US 5210701 A	19930511	15	Apparatus and method for designing integrated circuit modules	716/1

	Document ID	Issue Date	Pages	Title	Current OR
39	US 4720256 A	19880119	88	Hot isostatic press apparatus	425/78
40	NN9211335	19921101	NA	Highly Parallel Flow to Reduce Hydraulic Resistance of Heat Exchangers.	

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   08sep03 13:08:15 User267149 Session D972.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2003/Aug W5
         (c) 2003 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2003/Sep W1
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  File   8:Ei Compendex(R)  1970-2003/Aug W5
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         (c) 2003 ProQuest Info&Learning
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  File  94:JICST-EPlus  1985-2003/Sep W1
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  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
         (c) 2003 The HW Wilson Co.
  File 144:Pascal  1973-2003/Aug W5
         (c) 2003 INIST/CNRS
  File 305:Analytical Abstracts  1980-2003/Aug W3
         (c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Aug
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200357
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/May(Updated 030902)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	20942	ROUT???????(3N)(PROGRAM????? OR CONNECT????????)
S2	1334134	(INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?
S3	9009	(EMBED???????? OR ENCLOS????? OR MICROPORCESS??????)(3N)CORE? ?
S4	24315	(HORIZONTAL?????? OR VERTICAL????? OR DISSIMILAR???? OR DIFFERENT????? OR VARIOUS???? OR COMPROMIS????? OR ONE OR FIRST OR TWO OR SECOND)(3N)PITCH??????
S5	23391	INTERCONNECT?????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S6	18485	PROGRAMMAB??????()LOGIC()DEVICE? ? OR PLD OR PLDS
S7	25662	PROGRAMMAB??????(3N)LOGIC
S8	37719	S6:S7
S9	18543	FPGA OR FIELD()PROGRAMMAB????()GATE()ARRAY
S10	8212	LOGIC????(3N)BLOCK? ? OR CLG OR CLGS
S11	380	PROGRAMMAB?????(1N)(INPUT OR IN()PUT OR OUTPUT OR OUT()PUT-)(1N)BLOCK? ? OR IOB OR IOBS
S12	7559	S2 AND S8
S13	1250	S12 AND S9
S14	165	S13 AND S10
S15	6	S14 AND S11
S16	4	RD (unique items)
S17	159	S14 NOT S15
S18	14	S17 AND S1
S19	14	RD (unique items)
S20	145	S17 NOT S18
S21	0	S20 AND S1
S22	145	S20 AND S2
S23	1	S22 AND S5
S24	144	S22 NOT S23
S25	0	S24 AND S4
S26	144	S24 AND S8
S27	46	S26 AND S6
S28	30	S27 AND S7
S29	30	S28 AND S2
S30	30	RD (unique items)
S31	30	S30 AND (S9 OR S10 OR S11)
S32	16	S27 NOT S28
S33	0	S32 AND S4
S34	16	RD S32 (unique items)

16/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4476933 INSPEC Abstract Number: B9310-1270F-013, C9310-5240-013
Title: FIR filters with field-programmable gate arrays
Author(s): Mintzer, L.
Journal: Journal of VLSI Signal Processing vol.6, no.2 p.119-27
Publication Date: Aug. 1993 Country of Publication: Netherlands
CODEN: JVSPED ISSN: 0922-5773
U.S. Copyright Clearance Center Code: 0922-5773/93/$5.00
Language: English
Abstract: Distributed arithmetic techniques are the key to efficient implementation of DSP algorithms in FPGAs. The distributed arithmetic process is briefly described. A representative DSP design application in the form of an eight tap FIR filter is offered for the Xilinx XC3042 field **programmable logic** array (**FPGA**). The design is presented in sufficient detail-from filter specifications via filter design software through detailed logic of salient data and control functions to obtain a realistic placing and routing of configurable **logic block** (CLBs) and in/out block (**IOBs**) components for simulation verification and performance evaluation vis-a-vis commercially available dedicated eight tap FIR filter **chips**.
Subfile: B C

16/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05350278
E.I. No: EIP99094765909
Title: Single-**chip FPGA** implementation of the Data Encryption Standard (DES) algorithm
Author: Wong, K.; Wark, M.; Dawson, E.
Corporate Source: Queensland Univ of Technology, Queensland, Aust
Conference Title: Proceedings of the IEEE GLOBECOM 1998 - The Bridge to the Global Integration
Conference Location: Sydney, NSW, Aust Conference Date: 19981108-19981112
E.I. Conference No.: 55358
Source: Conference Record / IEEE Global Telecommunications Conference v 2 1998. p 827-832
Publication Year: 1998
CODEN: CRIEET
Language: English
Abstract: This paper describes a single **chip** implementation of the Data Encryption Standard (DES) using Xilinx XC4000 series **Field Programmable Gate Array** technology under the XACTstep design flow integration system. The implementation details for key scheduling, sboxes, permutations and the round-function are described. The design process included schematic design, functional and timing simulation and design verification. The final design used 224 Combinational **Logic Blocks** (CLBs) and 54 Input/Output Blocks (**IOBs**) and has an encryption speed of 26.7 Mbps. (Author abstract) 8 Refs.

16/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015089887
WPI Acc No: 2003-150405/200315
XRPX Acc No: N03-118726
Logic interface simplification system in **FPGA chip**, isolates intra-**programmable logic blocks** routing from memory address, data and control lines
Patent Assignee: STMICROELECTRONICS LTD (SGSA)
Inventor: BAL A
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1271783	A2	20030102	EP 200213243	A	20020617	200315	B
US 20030005402	A1	20030102	US 2002186314	A	20020628	200315	

Priority Applications (No Type Date): IN 2001729 A 20010629
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1271783	A2	E	11	H03K-019/177	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20030005402	A1			G06F-017/50	

Abstract (Basic): EP 1271783 A2
Abstract (Basic):
NOVELTY - A logic interface isolates the intra-**programmable logic blocks** (PLB) routing from memory address, data and control lines. The PLB and the input-output resource are connected to an embedded memory or RAM using a direct interconnection.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for interface simplification method.
USE - For simplifying logic interface between embedded memory, **programmable logic blocks** and **input**-output resources in **FPGA chip**.
ADVANTAGE - Eliminates the switch pattern interface between general routing and memories thereby obtaining simplified architecture.
DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram the single port memory with multiplexers and demultiplexers.
pp; 11 DwgNo 3/5

16/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014884601
WPI Acc No: 2002-705307/200276
XRPX Acc No: N02-555933
Programmable logic device e.g. **FPGA** includes amplitude/phase encoder to encode stream of multibit values of signal from input-output block, such that multibit values are encoded in different levels of amplitude and phase
Patent Assignee: XILINX INC (XILI-N)
Inventor: LESEA A H
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6437713	B1	20020820	US 2000684211	A	20001006	200276	B

Priority Applications (No Type Date): US 2000684211 A 20001006

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6437713	B1		16	H03M-007/00	

Abstract (Basic): US 6437713 B1

Abstract (Basic):

NOVELTY - The **logic** device includes a **programmable** interconnect structure which is configured to couple selected one of **logic blocks** and input-output blocks (**IOBs**). An amplitude/phase encoder (6), on receiving a signal from one of the **IOB**, encodes a stream of multibit values, each value having at least three bits, such that the multibit values are encoded in at least four different levels of amplitude and in at least four different phases.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **integrated circuit.**

USE - E.g. **FPGA integrated circuit** (claimed) such as SRAM based **FPGA** in **IC** package.

ADVANTAGE - Makes better use of input-output terminals by both amplitude and phase encoding a stream of multibit digital values into a single data signal.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of amplitude/phase encoder in **programmable logic device.**

Amplitude/phase encoder (6)

pp; 16 DwgNo 3/11

o matching display code(s) found in file(s): 65

18/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04364502
E.I. No: EIP96033112584
Title: Aspects of routability, capacity and speed in CPLDs & FPGAs
Author: Kapusta, Rich
Source: Australian Electronics Engineering v 29 n 2 Feb 1996. p 72-74
Publication Year: 1996
CODEN: AUEEB5 ISSN: 0004-9042
Language: English
Abstract: **Programmable logic devices** are leaping ahead in complexity and size. When selecting the right logic device for a job the designer needs to consider several factors. A look at some necessary considerations for using CPLDs and FPGAs is presented. It is shown that the capability of a **programmable logic device** depends on its resources, one major resource consideration being how signals are routed between **logic blocks** and I/O pins. A second major resource to consider are the characteristics of the **logic blocks**. Meanwhile, because of the size of the logic cells, the logic in an **FPGA** is typically more versatile than that in a CPLD, although the degree of fineness varies from supplier to supplier. In any case, the logic flexibility of an **FPGA** comes at a price. An **FPGA** cannot provide fixed delays and may be more complicated to use than a CPLD, although good design software should make such problems transparent to the user.

18/3,AB/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03473544
E.I. Monthly No: EIM9208-042867
Title: Optimization of **field-programmable** gate **array logic block** architecture for speed.
Author: Singh, Satwant; Rose, Jonathan; Lewis, David; Chung, Kevin; Chow, Paul
Conference Title: Proceedings of the IEEE 1991 Custom Integrated Circuits Conference
Conference Location: San Diego, CA, USA Conference Date: 19910512
E.I. Conference No.: 16672
Source: Proceedings of the Custom Integrated Circuits Conference. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 91CH2994-2). p 6p
Publication Year: 1991
CODEN: PCICER ISSN: 0886-5930 ISBN: 0-7803-0015-7
Language: English
Abstract: The authors explore the effect of the choice of **logic block** on the speed of a **field-programmable gate array** (**FPGA**). A set of logic circuits was implemented as FPGAs, each using a different **logic block**, and the speed of the implementation was measured. While the result depends on the delay of **programmable routing**, experiments indicate that wide input PLA (**programmable logic** array)-style AND-OR gates, four- and five-input lookup tables, and certain multiplexer configurations produce

the lowest total delay over the important values of routing delay. Furthermore, significant gains in performance (from 10% to 41% reduction in total delay) can be achieved by connecting a small number of **logic blocks** together using hard-wired connections. 12 Refs.

18/3,AB/3 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01478119 AADAAIMM04118
A GENERALIZED PROBABILISTIC MODEL TO PREDICT THE **ROUTABILITY** OF **FIELD-PROGRAMMABLE GATE ARRAY**-BASED APPLICATIONS
Author: NARDA, SANJAY
Degree: M.SC.
Year: 1995
Corporate Source/Institution: UNIVERSITY OF GUELPH (CANADA) (0081)
Source: VOLUME 34/03 of MASTERS ABSTRACTS.
PAGE 1205. 102 PAGES
ISBN: 0-612-04118-2

This thesis is an investigation of the effects of the routing architecture of a **Field-Programmable Gate Array** (**FPGA**) on the routability of an application. FPGAs are user-programmable **integrated circuits** that combine the benefits of gate arrays and **programmable logic devices**. The **routing** architecture of an **FPGA** is one of its key components. It comprises of the user-programmable switches and wiring segments that connect the **FPGA**'s Combinational **Logic Blocks** (CLBs). Routability is defined as the probability that a given circuit can be routed successfully on a target **FPGA**.

A generalized probabilistic model has been developed for routability prediction. Its purpose is to enable the user to assess the chances of routing an application successfully onto an **FPGA**, without going through the time-consuming process of placing and routing, and then discovering that the application is not routable. It is generalized in the sense that it is applicable to a wider range of architectures as compared to earlier attempts. It has also been enhanced to predict the routability for applications with timing constraints, and for cases in which more than one application is to be implemented on a single **FPGA**. A time-saving computational feature has also been added, which cuts down routability prediction times enormously, without significantly sacrificing accuracy.

18/3,AB/4 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15975726 PASCAL No.: 03-0119973
Modular, fabric-specific Synthesis for programmable architectures
FPL 2002 : field-**programmable logic** and applications : Montpellier, 2-4 September 2002
KOORAPATY Aneesh; PILEGGI Lawrence
GLESNER Manfred, ed; ZIPF Peter, ed; RENOVELL Michel, ed
Carnegie Mellon University, Pittsburgh PA 15213, United States
Reconfigurable computing is going mainstream. International conference, 12 (Montpellier FRA) 2002-09-02
Journal: Lecture notes in computer science, 2002, 2438 132-141

Language: English
Traditionally, programmable fabrics consist of look up table (LUT) based **programmable logic blocks** (PLBs). Typically, the PLBs are either homogeneous (consisting of LUTs of the same size), or heterogeneous (consisting of LUTs of varying sizes). To bridge the cost-performance gap between ASICs and FPGAs, several new **programmable logic** fabrics are employing highly heterogeneous PLB architectures, consisting of a combination of LUTs of varying sizes, MUXes, logic gates, and versatile local routing architectures. Currently, there are two possible approaches to Synthesis for such fabrics. In the generic Synthesis approach, the first step of technology mapping generates a netlist of functions that can be implemented by individual logic elements of a PLB, like LUTs, MUXes and logic gates. The second step of packing clusters these functions into groups of logic that can fit in a single PLB. The second approach constructs a library of certain PLB configurations (like a standard cell library) and performs library based technology mapping, followed by packing. In this paper, we show that both these approaches result in sub-optimal and uneven fabric utilization for two reasons: (a) a lack of fabric-specific knowledge; (b) a lack of integration between mapping and packing. We present a new, modular, Synthesis approach, consisting of a fabric-specific technology mapping algorithm which maps directly to the entire PLB, rather than individual logic elements. In this manner, the new approach integrates the steps of mapping and packing, resulting in higher fabric utilization. Using the highly heterogeneous eASIC PLB as an example, we demonstrate that our approach requires 22% and 24% fewer PLBs than the generic and library based Synthesis approaches, across a standard benchmark set. We also demonstrate the modularity of our approach, by comparing three PLB architectures. Our results show that highly heterogeneous PLBs are much more area efficient than homogeneous PLBs.

18/3,AB/5 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14819248 PASCAL No.: 00-0501832
A self-reconfigurable gate array architecture
FPL 2000 : field-**programmable logic** and applications : the roadmap to reconfigurable computing : Villach, 27-30 August 2000
SIDHU R; WADHWA S; MEI A; PRASANNA V K
HARTENSTEIN Reiner W, ed; GRUNBACHER Herbert, ed
Department of EE-Systems, University of Southern California, Los Angeles CA 90089, United States; Department of Mathematics, University of Trento, 38050 Trento (TN), Italy
Field-programmable logic and applications. International conference, 10 (Villach AUT) 2000-08-27
Journal: Lecture notes in computer science, 2000, 1896 106-120
Language: English
This paper presents an innovative architecture for a reconfigurable device that allows single cycle context switching and single cycle random access to the unified on-**chip** configuration/data memory. These two features are necessary for efficient self-reconfiguration and are useful in general as well-no other device offers both features. The enhanced context switching feature permits arbitrary regions of the **chip** to selectively context switch-its not necessary for the whole device to do so. The memory access feature allows data transfer between logic cells and

memory locations, and also directly between memory locations. The key innovation enabling the above features is the use of a mesh of trees based interconnect with **logic** cells and memory **blocks** at the leaf nodes and identical switches at other nodes. The mesh of trees topology allows a logic cell to be associated with a pair of switches. The logic cell and the switches can be placed close to the memory block that stores their configuration bits. The physical proximity enables fast context switching while the mesh of trees topology permits fast memory access. To evaluate the architecture, a point design with 8 x 8 logic cells was synthesized using a standard cell library for a 0.25 mu m process with 5 metal layers. Timing results obtained show that both context switching and memory access can be performed within a 10 ns clock cycle. Finally, this paper also illustrates how self-reconfiguration can be used to do basic **routing** operations of **connecting** two logic cells or inserting a logic cell by breaking an existing connection-algorithms (implemented as configured logic) to perform the above operations in a few clock cycles are presented.

18/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014035589
WPI Acc No: 2001-519802/200157
Related WPI Acc No: 2001-217813; 2002-253514; 2002-705091; 2003-287525
XRPX Acc No: N01-384827
Programmable **integrated circuit** for digital system, maintains equal number of connections between input multiplexer regions and primary conductors and between output multiplexer region and primary conductors
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: LYTLE C S; VEENSTRA K S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6181162	B1	20010130	US 9614942	P	19960405	200157	B
			US 9615122	P	19960410		
			US 97838398	A	19970403		
			US 983261	A	19980106		

Priority Applications (No Type Date): US 983261 A 19980106; US 9614942 P 19960405; US 9615122 P 19960410; US 97838398 A 19970403
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6181162	B1		15	H01L-025/00	Provisional application US 9614942 Provisional application US 9615122 Cont of application US 97838398

Abstract (Basic): US 6181162 B1
Abstract (Basic):
NOVELTY - An input multiplexer region (IMR) (504) programmably couples primary and secondary conductors to the **programmable logic** element (PLE) inputs. An output multiplexer region (OMR) (508) programmably couples the PLE outputs and several secondary conductors to several primary conductors. The number of programmable connections between IMR and primary conductors and between OMR and

primary conductors are equal.
USE - **Programmable logic IC** device for e.g. PAL, PLA, FPLA, **PLD**, EPLD, EEPLD, LCA, **FPGA** used for digital system.
ADVANTAGE - **Programmable logic device** architecture with highly **routable programmable** interconnect structure is achieved by coupling **programmable logic** element's input and output to two set of conductors by input and output multiplexer region respectively.
DESCRIPTION OF DRAWING(S) - The figure shows the connection of **logic** array **block** pair to GH interconnect.
Input multiplexer region (504)
Output multiplexer region (508)
pp; 15 DwgNo 7/9

18/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013717083
WPI Acc No: 2001-201307/200120
Related WPI Acc No: 1996-497044; 1998-321802; 2001-307405
XRPX Acc No: N01-143413
Programmable logic device integrated circuit used in digital system, has global **routing** block with **programmably connectable** vertical and horizontal conductors that couples **logic** array **block** and memory block
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: FARIA D F; LYTLE C S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6134166	A	20001017	US 95408504	A	19950322	200120 B
			US 96643809	A	19960506	
			US 9819423	A	19980205	

Priority Applications (No Type Date): US 96643809 A 19960506; US 95408504 A 19950322; US 9819423 A 19980205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6134166	A		22	G11C-007/00	CIP of application US 95408504
					Cont of application US 96643809
					CIP of patent US 5570040
					Cont of patent US 5757207

Abstract (Basic): US 6134166 A
Abstract (Basic):
NOVELTY - The **integrated circuit** comprises global **routing** block with **programmably connectable** vertical and horizontal conductors. The global routing **block** couples **logic** array **block** (201) and memory block (250) which is random access memory or first-in, first-out memory.
USE - E.g. **programmable** array logic (PAL), **programmable logic** array (PLA), field **programmable logic** array (FPLA), **programmable logic device** (**PLD**), erasable **programmable logic device** (EPLD), electrically erasable **programmable logic device**

(EEPLD), **logic** cell array (LCA), **field programmable gate array** (**FPGA**) used in communications, networks, digital video, digital telephony, multimedia and digital system such as programmed digital computer system, digital signal processing system, specialized digital switching network, general or special purpose computer, etc.

ADVANTAGE - Configuration information in a programmable circuit is updated or modified as needed, without requiring removal and installation of components or disassembly of system. Eliminates removal of programmable **IC** from circuit board and specially designed apparatus for programming **integrated circuits**.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of digital system incorporating **PLD integrated circuit**.

Blocks (201,250)

pp; 22 DwgNo 2/5

18/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013069115
WPI Acc No: 2000-240987/200021
XRPX Acc No: N00-181111

Test procedure of **field programmable gate array** for **integrated circuits**, involves comparing test pattern generated through two wires during test

Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE)
Inventor: ABRAMOVICI M; STROUD C E; WIJESURIYA S S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000055990	A	20000225	JP 99185794	A	19990630	200021	B

Priority Applications (No Type Date): US 98109123 A 19980630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000055990	A		13	G01R-031/28	

Abstract (Basic): JP 2000055990 A

NOVELTY - A test pattern generator (12) generates a test pattern and transmits through two wires (16,18). When built-in type self test is started, output of the wires are compared by a response analyzer (14) and the test result is displayed. DETAILED DESCRIPTION - The **programmable logic block** consists of the test pattern generator (12) and response analyzer (14). The subset of **programmable routing** network consists of wire during test (WUT) with wire segments (20,22,24,26,28,30,42,44,48,50) and group of interconnection points (31-39).

USE - For **integrated circuit** device.

ADVANTAGE - The entire routing network in a device, circuit board and system level is tested at high precision. DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of built-in type self test structure. (12) Test pattern generator; (14) Analyzer; (16,18) Wires; (20,22,24,26,28,30,42,44,48,50) Wire segments.

Dwg.1/15

18/3,AB/9 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012813579
WPI Acc No: 1999-619810/199953
Related WPI Acc No: 1998-427332; 1999-632406; 2001-463886; 2002-328426
XRPX Acc No: N99-457099

Logic blocks and **programmable routing** matrices architecture for reconfigurable **programmable logic device** e.g. **field programmable gate array**

Patent Assignee: XILINX INC (XILI-N)
Inventor: CARBERRY R A; JOHNSON R A; TRIMBERGER S M; WONG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5978260	A	19991102	US 95516808	A	19950818	199953	B
			US 98119534	A	19980720		

Priority Applications (No Type Date): US 95516808 A 19950818; US 98119534 A 19980720
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5978260	A		89	G11C-013/00	Cont of application US 95516808 Cont of patent US 5784313

Abstract (Basic): US 5978260 A
Abstract (Basic):

NOVELTY - Micro-registers simultaneously store intermediate state values corresponding to different configurations of a **programmable logic device** (**PLD**). Storage units provide read select signals to an output selector corresponding to a micro-register, to retrieve intermediate state values. The read select signals are selected and stored state values are used irrespective of the device configuration.

DETAILED DESCRIPTION - A memory controller provides write select signals to micro-registers to load the intermediate state values of the current device configuration into the micro-registers.

INDEPENDENT CLAIMS are also included for the following:

(a) **programmable logic device** operation method;

(b) **programmable logic device** configuration method;

(c) coupling method of output circuit to destination circuit; and

(d) low voltage interconnect structure for **integrated circuit**.

USE - For configurable **programmable logic** array e.g. **field programmable gate array** (**FPGA**).

ADVANTAGE - The switching of **PLD** between configurations is performed as flash reconfiguration, thereby reducing configurable **logic blocks** dynamically to implement a set of logic functions.

DESCRIPTION OF DRAWING(S) - The figure shows the configuration bit slice of **programmable logic device**.

pp; 89 DwgNo 2/64

18/3,AB/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012398035
WPI Acc No: 1999-204142/199917
XRPX Acc No: N99-150345
Increased **routing** capacity provided in **programmable logic device**
Patent Assignee: XILINX INC (XILI-N)
Inventor: DUONG K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5880598	A	19990309	US 97781251	A	19970110	199917	B

Priority Applications (No Type Date): US 97781251 A 19970110
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5880598	A		17	H03K-007/38	

Abstract (Basic): US 5880598 A
Abstract (Basic):
NOVELTY - Two sets of coupled modular routing resource tiles (116,114) are provided with conductive segments for coupling with corresponding set of configurable **logic blocks** (CLB). The tiles have programmable circuitry for selectively coupling to routing resources of the **logic blocks**. The tiles provide a modular communication path between input-output blocks (117).
DETAILED DESCRIPTION - The first group of tiles (116) comprises vertical modular tiles with vertical long line segment and quad line segments. The second set (114) comprises horizontal tiles with horizontal long line segments and quad line segments. The **logic blocks** comprise **logic** elements for implementing logic functions. A switch matrix interconnects individual signal lines of vertical and horizontal signal lines.
USE - For **field programmable gate array** (**FPGA**), complex **programmable logic device** (CPLD), application specific **integrated circuits** (ASIC).
ADVANTAGE - Avoids need for modification of CLB macrocell design so that existing libraries can be used to provide new, high density device families that have significant number of CLBs. Encounters signal congestion within programmable array.
DESCRIPTION OF DRAWING(S) - The figure illustrates interconnect structure of CLB interface with tiles.
Resource tiles (114,116)
Input-output blocks (117)
pp; 17 DwgNo 1B/8

18/3,AB/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010392011
WPI Acc No: 1995-293325/199538
XRPX Acc No: N95-221855
Field programmable gate arrays tile architecture to form **chips** in a variety of patterns - forms logic element and portion of routing matrix as part of tile, all made identical and joined to form arrays of

selectable size, with either direct **connections** or through **routing** matrix

Patent Assignee: XILINX INC (XILI-N)
Inventor: HOLEN V A; TAVANA D; YEE W K
Number of Countries: 018 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9522205	A1	19950817	WO 95US1554	A	19950207	199538	B
EP 698312	A1	19960228	EP 95909504	A	19950207	199613	
			WO 95US1554	A	19950207		
JP 8509344	W	19961001	JP 95521295	A	19950207	199705	
			WO 95US1554	A	19950207		
US 5682107	A	19971028	US 94222138	A	19940401	199749	
			US 96618445	A	19960319		
US 5883525	A	19990316	US 94222138	A	19940401	199918	
			US 96618445	A	19960319		
			US 97943890	A	19971003		

Priority Applications (No Type Date): US 94222138 A 19940401; US 94196914 A 19940215; US 96618445 A 19960319; US 97943890 A 19971003
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9522205	A1	E	79	H03K-019/177	
Designated States (National): JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 698312	A1	E	79	H03K-019/177	Based on patent WO 9522205
Designated States (Regional): DE FR GB					
JP 8509344	W		75	H03K-019/177	Based on patent WO 9522205
US 5682107	A		40	H03K-019/177	Cont of application US 94222138
US 5883525	A			H03K-007/38	Cont of application US 94222138
					Div ex application US 96618445
					Div ex patent US 5682107

Abstract (Basic): WO 9522205 A

Each core tile comprises a configurable **logic block** matrix and **programmable routing** matrix. Adjacent core tile configurable **logic block** matrices are connected. Inter-matrix lines connect the configurable **logic block** to the **programmable routing** matrix, and **routing** lines **connect programmable routing** matrix to **programmable routing** matrix in adjacent core tiles.

The core tiles may be identical or differ. Adjacent core tiles are positioned north, south, east and west of a core tile. Long lines extend horizontally through the core tile and at least one of the long lines is coupled to one of the inter-matrix lines. The routing matrix includes **routing** lines **connecting** from one tile to the next, and routing lines extend longer distances through several tiles or through the entire **chip**.

ADVANTAGE - Reduced cost, eliminates area while maximising configuration options.

Dwg.2B/30

Abstract (Equivalent): US 5682107 A

An **FPGA** tile architecture having a plurality of tiles, each said tile comprising:

a configurable **logic block** matrix, including **logic** circuitry;

a **programmable routing** matrix;

inter-matrix lines and lines directly connecting said configurable **logic block** matrix to said **programmable routing** matrix so as to provide for signal flow from said configurable **logic block** matrix to said **programmable routing** matrix and to provide for signal flow from said **programmable routing** matrix to said configurable **logic block** matrix; and

routing lines directly **connecting** said **programmable routing** matrix to **programmable routing** matrices in other said tiles, each said **routing** line being **programmably connectable** in said **programmable routing** matrix to another said routing line.

Dwg.2B/12

18/3,AB/12 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010213692
WPI Acc No: 1995-114946/199515
Related WPI Acc No: 1992-226160; 1993-205477; 1994-034424; 1995-193549; 1995-245861; 1997-064903; 1997-099627; 1998-192913; 2000-022347; 2000-430634
XRPX Acc No: N95-090710

Programmable application-specific **integrated circuit** for **field programmable gate array** - comprises **programmable routing** network, and **logic** cell integrated with **programmable** configuration network

Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: CHAN A K; CHUA H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5396127	A	19950307	US 91665103	A	19910306	199515 B
			US 92847382	A	19920306	
			US 92958866	A	19921008	
			US 94222726	A	19940329	

Priority Applications (No Type Date): US 91665103 A 19910306; US 92847382 A 19920306; US 92958866 A 19921008; US 94222726 A 19940329
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5396127	A		15	H03K-019/173	Cont of application US 91665103
					Cont of application US 92847382
					Cont of application US 92958866
					Cont of patent US 5122685

Abstract (Basic): US 5396127 A

The **field programmable gate array** includes a **programmable routing** network, a **programmable** configuration network integrated with the **programmable routing** network; and a logic cell integrated with the **programmable** configuration network. The **logic** cell includes four two-input AND gates, two six-input AND gates, three multiplexers, and a delay flipflop. The logic cell is a general purpose universal **logic** building **block** suitable for implementing most TTL and gate array macrolibrary functions.

A variety of functions are realizable with one cell delay, including combinational logic functions as wide as thirteen inputs, all Boolean transfer functions for up to three inputs, and sequential flipflop functions such as T, JK and count with carry-in.

ADVANTAGE - Higher speed, higher density, lower power dissipation and more flexible architecture.

Dwg.5/11

18/3,AB/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009950377
WPI Acc No: 1994-218090/199426
XRPX Acc No: N94-172182

Integrated circuit computing with dynamically configurable gate array - has reconfigurable execution unit which can be dynamically configured to implement variety of high level functions in hardware

Patent Assignee: METALITHIC SYSTEMS INC (META-N); NAT TECHNOLOGY INC (NATE-N); GILSON K L (GILS-I)
Inventor: GILSON K L
Number of Countries: 018 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9414123	A1	19940623	WO 93US11964	A	19931209	199426	B
US 5361373	A	19941101	US 92989236	A	19921211	199443	
EP 626084	A1	19941130	WO 93US11964	A	19931209	199501	
			EP 94903547	A	19931209		
JP 7503804	W	19950420	WO 93US11964	A	19931209	199524	
			JP 94514395	A	19931209		
EP 626084	A4	19950222	EP 94903547	A	19940000	199611	

Priority Applications (No Type Date): US 92989236 A 19921211
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9414123	A1	E	25	G06F-015/20	
Designated States (National): JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5361373	A		9	G06F-015/31	
EP 626084	A1	E	2	G06F-015/20	Based on patent WO 9414123
Designated States (Regional): DE FR GB					
JP 7503804	W		10	G06F-009/30	Based on patent WO 9414123
EP 626084	A4			G06F-015/20	

Abstract (Basic): WO 9414123 A

The **IC** computing device (10) has a dynamically configurable **Field Programmable Gate Array** (**FPGA**) (12). This gate array is configured to implement a RISC processor (14) and a reconfigurable instruction execution unit (16). Since the **FPGA** can be dynamically reconfigured, the RIEU (16) can be dynamically changed to implement complex operations in hardware rather than in time-consuming software routines.

USE/ADVANTAGE - **IC** appts. to dynamically configure gate array using microprocessor with reconfigurable instruction execution unit. Programmability of computing appts. makes is flexible and suited to handle large number of complex and different applications. Operates at

speeds that are orders of magnitude greater than traditional RISC or CISC computers.
Dwg.1/4

Abstract (Equivalent): US 5361373 A
Each of a number of dynamically configurable gate arrays have **programmable routing** resources for interconnecting I/O pads, I/O **blocks** and **programmable logic blocks**. The I/O **blocks**, the **logic blocks** and the **routing** resources are **programmed** to define an appropriate mode of operation for the gate array. A microprocessor is implemented within each gate array by the programming appts for processing instructions received from an external source. Reconfigurable instruction execution is implemented within each gate array using instructions from the microprocessor and the external source.
Manipulation and computation is performed on the data contained within th **logic blocks** of the gate arrays according to the information received. The reconfigurable execution is changed so an operation on data within the reconfigurable executer is carried out by circuits within th gate arrays after the reconfiguring is complete. A first of the dynamically configurable gate arrays is programmed to perform computations while the external source dynamically reconfigures a second dynamically configurable gate array.
Dwg.4/4

18/3,AB/14 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009754573
WPI Acc No: 1994-034424/199404
Related WPI Acc No: 1992-226160; 1993-205477; 1995-114946; 1995-193549; 1995-245861; 1997-064903; 1997-099627; 1998-192913; 2000-022347; 2000-430634
XRPX Acc No: N94-026815
Logic cell for **programmable**, application specific **integrated circuit** - has inputs connected via logic gates to multiplexers coupled to flip-flop
Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: BIRKNER J M; CHAN A K; CHUA H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5280202	A	19940118	US 91665103	A	19910306	199404 B
			US 92847137	A	19920306	
			US 9324986	A	19930302	

Priority Applications (No Type Date): US 91665103 A 19910306; US 92847137 A 19920306; US 9324986 A 19930302
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5280202	A		17	H03K-019/177	Cont of application US 91665103 Cont of application US 92847137 Cont of patent US 5122685 Cont of patent US 5220213

Abstract (Basic): US 5280202 A
The logic cell includes four two-input AND gates, two six-input AND

gates, three multiplexers, and a delay flipflop. The logic cell is a powerful general purpose universal **logic** building **block** suitable for implementing most TTL and gate array macrolibrary functions.

A variety of functions are realizable with one cell delay, including combinational logic functions as wide as thirteen inputs, all Boolean transfer functions for up to three inputs, and sequential flipflop functions such as T, JK and count with carry-in.

USE/ADVANTAGE - For **field programmable gate array** which includes programmable configuration network integrated with **programmable routing** network. Higher speed, higher density, lower power dissipation and more flexible architecture.

23/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011378773
WPI Acc No: 1997-356680/199733
XRPX Acc No: N97-296014
Variable **logic integrated circuit** for **programmable logic** LSI - arranges variable **logic block** and switch matrix in flag shape and sets up wiring area for connection between blocks using **multi layer interconnection** technique
Patent Assignee: HITACHI LTD (HITA)
Inventor: KUSUNOKI M; TAMBA N
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9148440	A	19970606	JP 95308733	A	19951128	199733	B
KR 97030762	A	19970626	KR 9656600	A	19961122	199828	
US 5825203	A	19981020	US 96747339	A	19961112	199849	

Priority Applications (No Type Date): JP 95308733 A 19951128
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9148440	A		18	H01L-021/82	
KR 97030762	A			H01L-027/00	
US 5825203	A			H03K-019/177	

Abstract (Basic): JP 9148440 A

The logic **integrated circuit** has variable **logic block** (PLB) with variable **logic** function and variable wiring cut. With variable wiring option, which are arranged on a semi-conductor **chip** (SUB) along vertical and horizontal direction respectively.

The variable **logic block** and a switch matrix (SMX) are arranged in the form of a checker flag. The wiring area for the connection between blocks are set up at variable **logic block** upper part, by applying the **multilayer interconnection** technique.

USE/ADVANTAGE - For use in FPLA, **FPGA**. Reduces occupancy area of switch matrix and **logic block**. Reduces **chip** size. Reduces number of switches between **logic blocks** Reduced signal propagation delay. Realizes operation at high speed.

Dwg.1/29

31/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7637112 INSPEC Abstract Number: B2003-06-1265B-094, C2003-06-5120-053
Title: Designing fail-safe systems with error correction capabilities using probabilistic analysis
Author(s): Pereira, M.; Soto, E.
Author Affiliation: R&D Digital Syst. Dept., Intelsis Sistemas Inteligentes S.A, Santiago de Compostela, Spain
Conference Title: Programmable Devices and Systems 2001 (PDS 2001). Proceedings volume from the 5th IFAC Workshop p.287-90
Editor(s): Hrynkiewicz, W.C.E.; Klosowski, P.
Publisher: Elsevier Sci, Kidlington, UK
Publication Date: 2002 Country of Publication: UK ix+309 pp.
ISBN: 0 08 044081 9 Material Identity Number: XX-2003-00126
Conference Title: Programmable Devices and Systems 2001. Proceedings volume from the 5th IFAC Workshop
Conference Sponsor: IFAC
Conference Date: 22-23 Nov. 2001 Conference Location: Gliwice, Poland
Language: English
Abstract: This paper proposes a general method for the design of fail-safe systems with error correction capabilities. A fail-safe system can detect an error in a transition between two states. With this method, errors produced in a transition between different states can be corrected by a design based on the analysis of probabilities. Analyzing the transition probabilities, an error corrector system can be built from the original unsafe system. This corrector system takes the form of a combinational **logic block** added to the unsafe system. In this method, the designer can adjust the complexity versus efficiency relationship of the corrector block.
Subfile: B C

31/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7522575 INSPEC Abstract Number: B2003-03-1265B-030, C2003-03-5120-022
Title: An automatic testing technique for **PLDs**
Author(s): Elsayed, A.; Elbably, M.; Elbolok, H.
Author Affiliation: Fac. of Eng., Helwan Univ., Cairo, Egypt
Conference Title: Proceedings of the Nineteenth National Radio Science Conference (NRSC'2002) (IEEE Cat. No.02EX567) p.413-20
Publisher: Alexandria Univ, Alexandria, Egypt
Publication Date: 2002 Country of Publication: Egypt 669 pp.
ISBN: 977 5031 72 9 Material Identity Number: XX-2002-02416
Conference Title: Proceedings of the Nineteenth National Radio Science Conference (NRSC'2002)
Conference Date: 19-21 March 2002 Conference Location: Alexandria, Egypt
Language: English
Abstract: The **programmable logic devices** (**PLDs**) are widely used in the hardware implementation of many designed circuits. Identifying the faulty row, which contains many configurable **logic blocks** (CLBs) was the aim of many researchers. A. new technique is

proposed in this research. The main aim of the proposed technique concentrates on identifying the location of the faculty CLB in **FPGA** (**field programmable gate array**) **chips**.
Subfile: B C
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31/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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7206862 INSPEC Abstract Number: B2002-04-1265B-052, C2002-04-5120-010
Title: History of **programmable logic devices**
Author(s): Perrin, B.
Author Affiliation: Lattice Semicond., Chertsey, UK
Journal: Elektronik Praxis no.22 p.36-41
Publisher: Vogel-Verlag,
Publication Date: 20 Nov. 2001 Country of Publication: Germany
CODEN: EKPXAM ISSN: 0341-5589
SICI: 0341-5589(20011120)22L.36:HPLD;1-M
Material Identity Number: E248-2001-023
Language: German
Abstract: Reviews the history of **Programmable Logic Devices** (**PLDs**) and Complex **Programmable Logic Devices** (CPLDs). Refers to the Series isp15KVE Configurable **Programmable Logic** from Lattice Semiconductors company, which operate on 3.3 V power supplies, and have up to 68 inputs. **Logic blocks** are described in detail. Also discusses the Series ispMACH-4A programmable device family fro Lattice, which have 3 nanosec propagation delay and can contain up to 192 macro-cells. Discusses the availability of efficient routing resources for FPGAs and CPLDs, and mentions programmable analogue circuits, which have EE (Electrically Erasable) memory. Notes that the market for ASICs is of the order or 20 billion dollars per annum. States that preferred geometry is based on 0.13 micron technology.
Subfile: B C
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31/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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6924493 INSPEC Abstract Number: B2001-06-1265B-038, C2001-06-5210B-021
Title: Practical logic synthesis for CPLDs and FPGAs with PLA-style **logic blocks**
Author(s): Yan, K.
Author Affiliation: ZettaCom, San Jose, CA, USA
Conference Title: Proceedings of the ASP-DAC 2001. Asia and South Pacific Design Automation Conference 2001 (Cat. No.01EX455) p.231-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xxxviii+676 pp.
ISBN: 0 7803 6633 6 Material Identity Number: XX-2001-00379
U.S. Copyright Clearance Center Code: 0 7803 6633 6/2001/$10.00
Conference Title: Proceedings of the ASP-DAC 2001. Asia and South Pacific Design Automation Conference 2001
Conference Sponsor: IEEE Circuits & Syst. Soc.; ACM SIGDA; IEICE (Inst. Electron., Inf. & Commun. Eng.); IPSJ (Inf. Process. Soc. Japan)
Conference Date: 30 Jan.-2 Feb. 2001 Conference Location: Yokohama,

Japan
Language: English
Abstract: In some modern FPGAs and CPLDs, PLA (**programmable logic** array)-style **logic blocks** can be used as the storage elements for improved logic density and performance. PLA-style **logic blocks** were originally deployed in the early **PLDs**. Due to recent research developments in the **FPGA** community, PLA-style **logic blocks** are becoming an effective storage alternative in FPGAs. This paper presents an approach with clustering and functional decomposition to implement the circuit using the minimum number of PLA-style **logic blocks** . One important feature is that it simultaneously considers the routing resource reduction for better circuit performance after place-and-route. In order to effectively use PLA-style **logic blocks** in large clusters, functional decompositions are used to decompose large clusters so that the encoding functions and base functions can be mapped into PLA-blocks. Furthermore, implicit representation of the crucial steps in the functional decomposition is used to consider: 1) number of inputs; 2) number of product terms; and 3) number of outputs required for the PLA-block synthesis. We have developed an algorithm called PLA-SynT that can be used in the logic synthesis flow for CPLDs and FPGAs with PLA-blocks. MCNC benchmarks are used to test PLA-SynT and the experimental results are compared with TEMPLA. PLA-SynT shows 10.24% improvement over TEMPLA, in terms of the number of PLA-blocks needed to implement the circuit. PLA-SynT also shows 14.41% improvement over EMB-Syn in circuit performances while maintaining comparable circuit areas.
Subfile: B C

31/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6666214 INSPEC Abstract Number: B2000-09-1265A-036, C2000-09-7410D-080
Title: Finding the right ASIC formula
Author(s): Diehl, S.
Journal: Portable Design vol.6, no.6 p.22-32
Publisher: PennWell Publishing,
Publication Date: June 2000 Country of Publication: USA
CODEN: PODEFP ISSN: 1086-1300
SICI: 1086-1300(200006)6:6L.22:FRAF;1-2
Material Identity Number: F261-2000-009
Language: English
Abstract: The race is on between ASIC technologies and the squeeze of shortening product cycles, but the cycles seem to stay a step ahead. Designers try every trick to get ahead, but with new portable technologies and wireless standards changing as fast as the product cycles, designers face not only increased time-to-market pressures but also exponentially greater hardware and software complexities. All major ASIC companies are now standardized on nonproprietary EDA tools, usually wrapping their own manufacturing technologies around the EDA software modules. In order to meet the relentlessly shortening design cycles, ASIC methodologies must bundle effective timing and power tools, **programmable logic blocks**, and integrated pipes into the manufacturing process.
Subfile: B C

31/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6509362 INSPEC Abstract Number: B2000-04-1265B-006, C2000-04-5210-002
Title: An approach for detecting multiple faulty **FPGA logic blocks**
Author(s): Wei Kang Huang; Meyer, F.J.; Lombardi, F.
Author Affiliation: Syst. State Key Lab., Fudan Univ., Shanghai, China
Journal: IEEE Transactions on Computers vol.49, no.1 p.48-54
Publisher: IEEE,
Publication Date: Jan. 2000 Country of Publication: USA
CODEN: ITCOB4 ISSN: 0018-9340
SICI: 0018-9340(200001)49:1L.48:ADMF;1-T
Material Identity Number: I071-2000-003
U.S. Copyright Clearance Center Code: 0018-9340/2000/$10.00
Language: English
Abstract: An approach is proposed to test **FPGA logic blocks** , including part of the configuration memories used to control them. The proposed AND tree and OR tree-based testing structure is simple and the conditions for constant testability can easily be satisfied. Test generation for only a single **logic block** is sufficient. We do not assume any particular fault model. Any number of faulty blocks in the **chip** can be detected. Members of the Xilinx XC3000, XC4000, and XC5200 families were studied. The proposed AND/OR approach was found to reduce the number of **FPGA** reprogrammings needed for testing by up to a factor of seven versus direct methods of multiple faulty block detection.
Subfile: B C

31/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

04287710 INSPEC Abstract Number: B9301-1265B-007, C9301-5120-003
Title: RAM-based logic arrays up density, cut delays
Author(s): Bursky, D.
Journal: Electronic Design vol.40, no.20 p.45-6, 48-9
Publication Date: 1 Oct. 1992 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
U.S. Copyright Clearance Center Code: 0013-4872/92/$1.00+.50
Language: English
Abstract: Combination coarse-grain/fine-grain logic arrays offer up to 24000 usable gates and the best performance of any alterable array. The newly developed CMOS RAM-based family of field-**programmable logic devices** includes five **chips** that range in capacity from 8000 to 48000 available (4000 to 24000 usable) gates and can operate in systems with clock rates of up to 70 MHz. The new five-**chip** family designed by Altera, called the FLEX (flexible-logic-element-matrix) 8000 family, is RAM-based making the **chips** in-system reconfigurable. The family is the company's first entry into the RAM-based logic arena. Building on previous EPROM- or EEPROM-based array architectures, the FLEX arrays provide a register-intensive architecture that packs from 452 to 2252 flip-flops-the largest numbers for any announced **FPGA**-and many I/O lines. Predictable, deterministic timing is also possible as a result of new high-performance **logic** building **blocks** and global wiring channels called FastTracks. The FastTracks keep the cross-**chip**

worst-case interconnection delays to just 9 ns.
Subfile: B C

31/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

03767347 INSPEC Abstract Number: B90075130, C91002978
Title: MACH family closes the gap between PALs and FPGAs
Author(s): von Bechen, P.
Author Affiliation: AMD GmbH, Munchen, West Germany
Journal: Elektronik Industrie vol.21, no.5 p.56, 58
Publication Date: May 1990 Country of Publication: West Germany
CODEN: EKIDAT ISSN: 0374-3144
Language: German
Abstract: Compared to **programmable** array **logic** (PAL) circuits, the field programmable arrays (**FPGA**) have a higher density of integration but are slower in operation. The new MACH (macro array CMOS high-speed) **chips** of AMD, comprising 900 to 3600 gates, bring the advantages of faster operation and the Dame ease of design as PALs. Like other **programmable logic devices**, the **chips** contain **programmable logic blocks**, interconnected by a programmable switching matrix, with a 1 or 2 ns delay, which is a tenfold improvement in the switching speed. The reason is that individual PAL groups do not need any buffer stages. The circuit of a MACH macrocell is shown.
Subfile: B C

31/3,AB/9 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06368855
E.I. No: EIP03187452891
Title: **Programmable logic** & hardware
Author: Williams, Al
Source: Dr. Dobb's Journal v 28 n 5 May 2003. p 70-75
Publication Year: 2003
CODEN: DDJTEQ ISSN: 1044-789X
Language: English
Abstract: A discussion was presented on programming of hardware with field programmable gate arrays (**FPGA**) and complex **programmable logic devices** (CPLD). **FPGA** contain myraid **logic blocks** and a **programmable** interconnect switch that could tie different blocks together. CPLD are arrays of macrocells that connect to each other and I/O through a programmable switch similar to that of an **FPGA**. (Edited abstract)

31/3,AB/10 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06160811
E.I. No: EIP02417137902
Title: **FPGA** 2002 Tenth ACN international symposium on

field-programmable gate arrays
Author: Anon (Ed.)
Conference Title: FPGA 2002: Tenth ACM International Symposium on Field-Programmable Gate Arrays
Conference Location: Monterey, CA, United States Conference Date: 20020224-20020226
E.I. Conference No.: 59914
Source: ACM/SIGDA International Symposium on Field Programmable Gate Arrays - FPGA 2002. 255p
Publication Year: 2002
Language: English
Abstract: The proceedings contains 26 papers from the **FPGA** 2002 Tenth ACM International Symposium on Field-Programmable Gate Arrays. Topics discussed include: interconnect enhancements for a high-speed **PLD** architecture; **FPGA** switch block layout and evaluation; a faster distributed arithmetic architecture for FPGAs; efficient circuit clustering for area and power reduction in FPGAs and integrated retiming and placement for field programmable gate arrays. (Edited abstract)

31/3,AB/11 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04070027
E.I. No: EIP95022559965
Title: Experiences in teaching ASIC design using xilinx **FPGA** and mentor graphics tools
Author: Lu, Shih-Lien
Corporate Source: Oregon State Univ, Corvallis, OR, USA
Conference Title: Proceedings of the 7th IEEE International ASIC Conference and Exhibit
Conference Location: Rochester, NY, USA Conference Date: 19940919-19940923
E.I. Conference No.: 42410
Source: Annual IEEE International ASIC Conference and Exhibit 1994. IEEE, Piscataway, NJ, USA,94TH0685-8. p 192-195
Publication Year: 1994
CODEN: PIAEF2 ISSN: 1063-0988
Language: English
Abstract: We have developed a new course on digital design using Xilinx' **FPGA** and Mentor Graphics' tools. This paper summarize the experience on preparation as well as teaching the course. (Author abstract) 23 Refs.

31/3,AB/12 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01784704 AADAAI9992847
CAD algorithms for field **programmable logic devices**
Author: Lee, Kok Kiong
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: The University of Texas at Austin (0227)
Source: VOLUME 61/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5960. 146 PAGES
ISBN: 0-493-01029-7

Field **Programmable Logic Devices** (FPLDs) are logic devices that allow users to program the devices after fabrication. Due to the programmability and low cost of these devices compared with custom design **chips** at low to medium volume, FPLDs are very popular in rapid system prototyping, logic emulation and reconfigurable computing.

In this dissertation, we describe the research results on some CAD algorithms for FPLDs. The scope includes technology mapping, routing, reconfiguration in multi-FPLD systems and **logic block** design. The two main types of FPLDs considered in this dissertation are Complex **Programmable Logic Devices** (CPLDs) and Field Programmable Gate Arrays (FPGAs).

We describe minimum area technology mapping results for two kinds of look up table (LUT) based **logic blocks** in FPGAs. The first type of **logic blocks** contain LUTs of different sizes that are independent. The second type contain LUTs that are connected. The problems are NP-complete for general network circuits. We show the first polynomial time minimum area technology mapping algorithms for tree circuits for both types of **logic blocks**. Experimental results show that the running times of the algorithms are very fast in practice and the mapping quality matches those of other non-tree-based algorithms that uses much more computation time.

We also consider routing for hierarchical CPLDs that have constraints on the routing topologies because of architectural and performance considerations. The constraints complicate routing and adaptations of ASIC or **FPGA** routers to this problem do not work well. We describe a novel router for this problem based on the Lagrangian Relaxation framework. This router is effective, solving a set of routing problems that commercial software failed to route. The router is also very fast.

In reconfigurable computing, circuits implemented on multi-**FPGA** systems have to be modified often. Since reconfiguring an **FPGA** is very time-consuming, our objective is to reduce the number of FPGAs to be reconfigured. This problem can be separated into a net addition (NAP) and a net deletion problem (NDP). NAP is a generalized case of the NP-complete Steiner Tree Problem. We prove that NDP for interesting and practical multi-**FPGA** layouts are also NP-complete. We describe an algorithm for solving this reconfiguration problem which handles both placement and inter-**FPGA** routing.

We also show some results on designing a new kind of **logic blocks** for FPGAs. We show how **logic blocks** with small number of programmable switches are designed. The area used are smaller than other designs. Mapping algorithms are also given.

31/3,AB/13 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05184312 JICST ACCESSION NUMBER: 02A0426749 FILE SEGMENT: JICST-E
Design Technologies and Design Automation of Electronic Systems. Proposal and Evaluation of a **Logic Block** Architecture for Reconfigurable **Logic**.
IIDA MASAHIRO (1); SUEYOSHI TOSHINORI (2)
(1) Kumamoto Univ., Graduate School of Sci. and Techol. (Doctoral Degree Program), JPN; (2) Kumamoto Univ., Fac. of Eng.
Joho Shori Gakkai Ronbunshi(Transactions of Information Processing Society of Japan), 2002, VOL.43,NO.5, PAGE.1181-1190, FIG.11, TBL.10, REF.15
JOURNAL NUMBER: Z0778AAZ ISSN NO: 0387-5806

UNIVERSAL DECIMAL CLASSIFICATION: 681.3:658.51 681.32
621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In this paper, we propose a **logic block** architecture of **programmable logic** that is suitable for reconfigurable computing. Our **logic block** contains configuration data cache for holding multiple contexts and the LUT (Look Up Table) that has the functions of multi-context and clustering. The context is a unit of configuration data for circuit. we evaluate implementation efficiency, implementation area and configuration data bits through mapping some benchmark circuits. As a result of the evaluation, the implementation density is improved up to about 2.5 times than the conventional **logic block** using 4-LUT by means of the configuration data cache. The implementation efficiency is improved about 6% by clustering of LUT. Moreover, the implementation area and the amount of the configuration data indicate minimum values respectively by means of the multi-context. (author abst.)

31/3,AB/14 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05071162 JICST ACCESSION NUMBER: 02A0191874 FILE SEGMENT: JICST-E
Proposal of a **Logic Block** Architecture for Reconfigurable **Logic**.
IIDA MASAHIRO (1); SUEYOSHI TOSHINORI (2)
(1) Kumamoto Univ., Graduate School of Sci. and Techol. (Doctoral Degree Program), JPN; (2) Kumamoto Univ., Fac. of Eng.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2001, VOL.101,NO.474(CPSY2001 75-80), PAGE.25-30, FIG.8, TBL.8, REF.10
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.37:681.325.6 621.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In this paper, we propose a **logic block** architecture of **programmable logic** that is suitable for reconfigurable computing. Our **logic block** contains configuration data cache(CDC) for holding multiple contexts and the LUT(Look Up Table) that have the functions of multi-context and clustering. It is in control of the contexts using two classes, which are both the LUT and the CDC, so that runtime reconfiguration and partial reconfiguration are possible of realization. We evaluate implementation efficiency, implementation area and configuration data bits through mapping some benchmark circuits. As a result of the evaluation, our **logic block** can be carried on the CDC that the capacity is 2,048 bits on condition that the delay is level with 4-LUT. The implementation density is improved up to 3 times than the conventional **logic block** using 4-LUT by means of the configuration data cache. The implementation efficiency is improved about 8% by clustering of LUT. Moreover, the implementation area and the amount of the configuration data indicate minimum values respectively by means of the

multi-context. (author abst.)

31/3,AB/15 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2256498 H.W. WILSON RECORD NUMBER: BAST01013635
Features and benefits of ALU-based **programmable logic**
Rupp, Charles R;
Electronic Engineering v. 73 no889 (Feb. 2001) p. 44-5
DOCUMENT TYPE: Feature Article ISSN: 0013-4902

ABSTRACT: The writer argues in support of a **FPGA** architecture based on an arithmetic **logic** unit (ALU). **Programmable logic block** units using ALUs are very well suited for use as embedded logic in system-on-a-**chip** components. The higher-level ALU and cluster structure allows a family of arrays with different width, height, and I/O characteristics. The configuration data for such a **logic block** can be accessed through a ROM interface or an internal processor bus, allowing the configuration of the **programmable logic** to be changed dynamically. ALU based **programmable logic** offers 2 levels of programmability and permits design implementation using the same design flow used for custom logic.

31/3,AB/16 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1248321 H.W. WILSON RECORD NUMBER: BAST95044073
Embedded configurable memory and logic boost **FPGA** functionality
AUGMENTED TITLE: FLEX 10K family from Altera Corp.
Bursky, Dave;
Electronic Design v. 43 (July 10 '95) p. 152
DOCUMENT TYPE: Product Evaluation ISSN: 0013-4872

ABSTRACT: The FLEX 10K family of field-**programmable logic devices** from Altera Corp., San Jose, California, are targeted at memory-intensive applications that also require the flexibility of **programmable logic**. The arrays offer designers an architecture that will support logic densities that can reach 100,000 gates per **chip**. Initially, there will be 7 arrays in the family, with complexities ranging from 72 **logic** array **blocks** (LABs) and 3 embedded array blocks (EABs) to 676 LABs and 13 EABs. Prices depend on package option and quantity.

31/3,AB/17 (Item 3 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1115607 H.W. WILSON RECORD NUMBER: BAST93047744
Special section on field programmable gate arrays
Proceedings of the IEEE v. 81 (July '93) p. 1011-83
DOCUMENT TYPE: Feature Article ISSN: 0018-9219

ABSTRACT: A special section examines **field programmable**

gate array (**FPGA**) technology. FPGAs are electrically programmable **integrated circuits** that provide high **integration** previously possible only with mask programmable gate arrays and traditional PLA based **programmable logic devices**. The special section is comprised of 4 papers. The first paper provides a survey of existing **FPGA** architecture and programming technologies and a classification of FPGAs based on the granularity of their **logic blocks**. The second and third papers consist of detailed descriptions of the 2 most popular FPGAs, the Xilinx SRAM-based **FPGA** and the Actel antifuse-based architecture. The fourth paper provides a comprehensive survey pf recent research on logic synthesis specifically targeted at FPGAs.

31/3,AB/18 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015226612
WPI Acc No: 2003-287525/200328
Related WPI Acc No: 2001-217813; 2001-519802; 2002-253514; 2002-705091
XRPX Acc No: N03-228407
Logic block for **integrated circuit**, has input and output multiplier regions which **programmably** couples output from **logic** elements and global interconnects and provides it to other global interconnect
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: LYTLE C S; VEENSTRA K S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6492834	B1	20021210	US 9614942	P	19960405	200328 B
			US 9615122	P	19960410	
			US 97838398	A	19970403	
			US 983261	A	19980106	
			US 2001687215	A	20010201	

Priority Applications (No Type Date): US 2001687215 A 20010201; US 9614942 P 19960405; US 9615122 P 19960410; US 97838398 A 19970403; US 983261 A 19980106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6492834	B1		16	H03K-019/177	Provisional application US 9614942 Provisional application US 9615122 Cont of application US 97838398 Cont of application US 983261 Cont of patent US 6181162

Abstract (Basic): US 6492834 B1
Abstract (Basic):
NOVELTY - A Clos network has an input multiplexer region (504) programmably couples output of the logic elements (LE) (300) and global horizontal interconnects (GH) (210), and provides to input of LE's, pins (516) and global vertical interconnects (GV) (220). An output multiplexer region (508) of Clos network couples output from LE's, GV and pins and provides it to GH.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **integrated circuit**.

USE - For **programmable logic device integrated circuit** (claimed) e.g. **programmable** array **logic** (PAL), **programmable logic** array (PLA), field PLA, erasable **PLD**, electrically erasable **PLD**, logic cell array (LCA), **field programmable gate array** (**FPGA**).

ADVANTAGE - The Clos network enable region of switching network with probable routability with minimum interconnect and other resources.

DESCRIPTION OF DRAWING(S) - The figure shows the **block** diagram of **logic** array **block**.

GH (210)
GV (220)
LE (300)
input and output multiplexer regions (504,508)
pins (516)
pp; 16 DwgNo 5/9

31/3,AB/19 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015187095
WPI Acc No: 2003-247628/200324
XRPX Acc No: N03-196836

Integrated circuit fault insertion system for testing diagnostic software, applies normal signal to circuit node when fault identification register output signal is not asserted

Patent Assignee: DAVIES B S (DAVI-I)
Inventor: DAVIES B S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020199134	A1	20021226	US 2001888025	A	20010625	200324	B

Priority Applications (No Type Date): US 2001888025 A 20010625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020199134	A1		8	H04L-001/22	

Abstract (Basic): US 20020199134 A1
Abstract (Basic):

NOVELTY - A fault identification register (FIR) receives a FIR code from a source of register values and a FIR decoder (4) decodes the received code and asserts a FIR decode block output signal when a logic output signal is asserted. A **logic block** applies a normal signal to a circuit node when the FIR output signal is not asserted and applies a test signal to the circuit node when the FIR signal output signal is asserted.

USE - For insertion of faults e.g. permanent fault, transient fault, intermittent fault, stuck-at type fault in **integrated circuits** e.g. **field programmable gate array, programmable logic device**, LSI circuit, VLSI circuit, ULSI circuit, ASIC for testing diagnostic software.

ADVANTAGE - The faults can be induced without the need of high accessible circuit nodes.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of

the **integrated circuit** fault insertion system.
decoder (4)
pp; 8 DwgNo 1/4

31/3,AB/20 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015171444
WPI Acc No: 2003-231972/200323
XRPX Acc No: N03-184627
Programmable logic function **block** for reconfigurable devices, has logic function generator to generate logical output signal from three input signals according to logical function selected from input/output logical functions
Patent Assignee: NEC CORP (NIDE)
Inventor: NAKAYA S
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1271474	A1	20030102	EP 200213978	A	20020625	200323 B
CA 2391798	A1	20021225	CA 2391798	A	20020625	200323
US 20030001613	A1	20030102	US 2002177180	A	20020624	200323
JP 2003084967	A	20030320	JP 2002179301	A	20020620	200330

Priority Applications (No Type Date): JP 2002179301 A 20020620; JP 2001191770 A 20010625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1271474	A1	E	176	G11B-005/03	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
CA 2391798	A1	E		H03K-019/00	
US 20030001613	A1			H03K-019/173	
JP 2003084967	A		104	G06F-007/00	

Abstract (Basic): EP 1271474 A1
Abstract (Basic):
NOVELTY - A logic function generator generates logical output signal from three input signals according to the logical function selected from input/output logical functions. Three signal generators generate respective signals from the logical input signal. A selector selects one of the three signals to produce a carry output signal. An exclusive OR circuit produces an ORed result from the logical output.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Function cell;
(2) Combined function block;
(3) Complex function block;
(4) **Integrated circuit** comprising function blocks;
(5) N bit 4-2 adder;
(6) N-bit 4AND4-2 adder;
(7) Multiplier; and
(8) Barrier shifter.
USE - **Programmable logic** function **block** for reconfigurable devices such as **programmable logic device, field programmable gate array.**

ADVANTAGE - Provides a function block that constitutes a compact high speed multiplier.
pp; 176 DwgNo 0/107

31/3,AB/21 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014852385
WPI Acc No: 2002-673091/200272
XRPX Acc No: N02-532086
Field **programmable logic device integrated circuit** has interface cells each having output buffer coupled to respective output node of clock tree coupled to DLL circuit, to drive signal off-**chip**
Patent Assignee: XILINX INC (XILI-N)
Inventor: BAPAT S; HUNG L C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6429715	B1	20020806	US 2000482741	A	20000113	200272	B

Priority Applications (No Type Date): US 2000482741 A 20000113
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6429715	B1		14	G06F-001/04	

Abstract (Basic): US 6429715 B1
Abstract (Basic):
NOVELTY - A delay-locked loop (DLL) circuit (107) has an output coupled to an input node of balanced clock tree (108). Each of interface cells (127-130) arranged along an edge of the **integrated circuit** (**IC**), has an output buffer (132) to drive signal off-**chip**. The input of each buffer is coupled to respective output nodes of the clock tree. The cells are arranged in row between a matrix of configurable **logic block** and edge of the **IC**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for clock signal de-skewing system.
USE - Field **programmable logic device integrated circuit** for de-skewing of clock signals for off-**chip** devices such as RAM devices.
ADVANTAGE - The single **field programmable gate array** (**FPGA**) design drives different external RAM devices in different board level implementations, which does not involve designing complex balanced clock trees.
DESCRIPTION OF DRAWING(S) - The figure shows a simplified top-down view of the clock signal de-skewing system.
Delay-locked loop circuit (107)
Clock tree (108)
Interface cells (127-130)
Output buffer (132)
pp; 14 DwgNo 9/12

31/3,AB/22 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014523496
WPI Acc No: 2002-344199/200238
XRPX Acc No: N02-270818
Information processing system for ASIC manufacture, arranges functionally dependent **logic blocks** in same row of programmable CTS, based on prestored block reconfiguration conditions
Patent Assignee: FUJI XEROX CO LTD (XERF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002007161	A	20020111	JP 2000191544	A	20000626	200238	B

Priority Applications (No Type Date): JP 2000191544 A 20000626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002007161	A		10	G06F-011/00	

Abstract (Basic): JP 2002007161 A
Abstract (Basic):
NOVELTY - The information processing system arranges several **logic blocks** in a **programmable** CTS (26), based on prestored circuit information for reconfiguration conditions of the **logic blocks**, so that functionally dependent blocks are arranged in the same row of the CTS.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for information processing method.
USE - For manufacturing application specific **integrated circuits** for use in **field programmable gate array** (**FPGA**), **programmable logic device** (**PLD**).
ADVANTAGE - As functionally dependent **logic blocks** are arranged in the same row of a programmable CTS, the number of reconfigurable blocks is reduced and hence reconfiguration time is also reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a conceptual diagram of the arrangement of **logic blocks** in a **programmable** CTS. (Drawing includes non-English language text).
Programmable CTS (26)
pp; 10 DwgNo 6/9

31/3,AB/23 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014341854
WPI Acc No: 2002-162557/200221
XRPX Acc No: N02-123943
Computer subsystem architecture in **programmable logic devices**, has monolithic substrate for coupling onto PCB, with conductors extending between non-volatile memory circuit and **programmable logic** circuit
Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: CHANG B S; CHHOR K S; LACEY T M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6215689	B1	20010410	US 99442851	A	19991118	200221 B

Priority Applications (No Type Date): US 99442851 A 19991118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6215689	B1		12	H01L-021/70	

Abstract (Basic): US 6215689 B1
Abstract (Basic):

NOVELTY - Computer subsystem architecture has non-volatile memory circuit, and **programmable logic** circuit (44) which are coupled on a monolithic substrate. Monolithic substrate has conductors (42) extending between non-volatile memory circuit (46) and **programmable logic** circuit and is adapted for coupling onto a printed circuit board.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) **Programmable logic device;**

(b) Volatile memory cell configuring method

USE - In **programmable logic devices** like **programmable** read only memory (PROM), field **programmable logic** arrays (FPLA), **programmable** array **logic** device (PAL), field **programmable** gate arrays (**FPGA**), etc.

ADVANTAGE - **Programmable logic device** maintains its programmed status even when power is switched OFF, as the non-volatile memory **integrated circuit** is separated from the **programmable logic integrated circuit** bearing volatile, high speed **logic blocks**. Interconnection between two **integrated circuits** occurs solely upon the substrate and does not involve the use of printed conductors, thus freeing the printed conductors for other applications.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of volatile memory cells arranged within **logic blocks** of a **programmable logic integrated circuit.**

Conductors (42)

Programmable logic circuit (44)

Non-volatile memory circuit (46)

pp; 12 DwgNo 4/9

31/3,AB/24 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013979672
WPI Acc No: 2001-463886/200150
Related WPI Acc No: 1998-427332; 1999-619810; 1999-632406; 2002-328426
XRPX Acc No: N01-343942

Time multiplexing method for **programmable logic devices**, involves dynamic reconfiguration of **logic blocks** and routing matrices

Patent Assignee: XILINX INC (XILI-N)
Inventor: CARBERRY R A; JOHNSON R A; TRIMBERGER S M; WONG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6263430	B1	20010717	US 95516808	A	19950818	200150 B

	US 971156	A	19971230
	US 99363940	A	19990729

Priority Applications (No Type Date): US 95516808 A 19950818; US 971156 A 19971230; US 99363940 A 19990729

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6263430	B1		85	G06F-009/00	Cont of application US 95516808 Cont of application US 971156 Cont of patent US 5784313 Cont of patent US 5959881

Abstract (Basic): US 6263430 B1

Abstract (Basic):

NOVELTY - A **programmable logic device** (**PLD**) comprises **programmable** memory cells that form a memory slice. Portions of slices are configured as data memory or user data memory. The **PLD** switches between configurations sequentially, by random access, or on demand from an internal or external signal. A memory access port couples between configurable **logic blocks** (CLB) for loading new on/off **chip** data.

USE - Reconfiguring Filed Programmable Gate Arrays (**FPGA**).

ADVANTAGE - Reduced number of CLBs required due to reuse by flash reconfiguration.

pp; 85 DwgNo 42/64

31/3,AB/25 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013965930

WPI Acc No: 2001-450144/200148

Related WPI Acc No: 1999-263250

XRPX Acc No: N01-333143

Programmable logic device e.g. field programmable gate arrays for **integrated circuits**, has pair of predriver transistor sets connected to control electrodes of corresponding driver transistors

Patent Assignee: ALTERA CORP (ALTE-N)

Inventor: CLIFF R G; REDDY S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6239613	B1	20010529	US 96587875	A	19960110	200148	B
			US 98169207	A	19981009		

Priority Applications (No Type Date): US 96587875 A 19960110; US 98169207 A 19981009

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6239613	B1		19	H03K-019/00	Div ex application US 96587875 Div ex patent US 5894228

Abstract (Basic): US 6239613 B1

Abstract (Basic):

NOVELTY - Predriver transistors (627,635) of a tristate driver (520) are connected between voltage source (622) and control electrode

of driver transistor (620). Predriver transistors (630,637) are connected in between the control electrodes of driver transistors (620,625), and predriver transistors (633,639) are coupled between control electrode of driver transistor (625) and voltage source (627).

DETAILED DESCRIPTION - The **programmable logic device** includes multiplexer comprising an input coupled to **logic** array **block** such that the multiplexer selectively couples the **logic** array **block** to one of the multiple conductors. A tristate driver (520) coupling **logic** array **block** to one of another set of conductors in dynamically controlled by **logic** in **logic** array **block**. The tristate driver includes data input (RSEL) (647), enable input (645), driver transistors (620,625) and pair of predriver transistor sets (627,630,633 and 633,637,639). The driver transistor (620) is coupled between voltage source (622) and output node (B0) and transistor (625) is coupled between output node and voltage source (627). The control electrode of predriver transistors (627,630) are connected to inversion of enable input and control electrode of predriver transistor (633) is connected to enable input. The control electrodes of predriver transistors (635,639) are connected to data input (RSEL) and control electrode of predriver transistor (637) is coupled to enable input.

INDEPENDENT CLAIMS are also included for the following:

(a) System having **programmable logic device**;

(b) Programmable **integrated circuit**;

(c) System having programmable **integrated circuit**

USE - E.g. **programmable** array logic (PAL), **programmable logic** arrays (PLA), erasable **programmable logic devices** (EPLD), electrically erasable **programmable logic devices** (EEPLD), **logic** cell arrays (LCA) and field programmable gate arrays (**FPGA**), for **integrated circuits**.

ADVANTAGE - By coupling predriver transistors to corresponding driver transistors, greater utilization and flexibility in using programmable and global interconnect structures of **programmable logic device** are enabled and hence performance and operating characteristics of **programmable logic device** are improved with increased transient response.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic circuit diagram of tristate driver.

Tristate driver (520)

Driver transistors (620,625)

Voltage source (622,627)

Predriver transistors (627,635,630,637,633,639)

Enable input (645)

Data input (647)

pp; 19 DwgNo 6/6

31/3,AB/26 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013750158

WPI Acc No: 2001-234387/200124

XRPX Acc No: N01-167570

Programmable logic device for **field programmable gate array** has global clock network has distributed clock terminals connected to **logic-block** clock

terminals to send clock signal to each configurable logic
Patent Assignee: XILINX INC (XILI-N)
Inventor: GOETTING F E; HUNG L C; SCHULTZ D P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6191613	B1	20010220	US 99363941	A	19990729	200124 B

Priority Applications (No Type Date): US 99363941 A 19990729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6191613	B1		10	H03K-019/177	

Abstract (Basic): US 6191613 B1
Abstract (Basic):

NOVELTY - A sequencer (240) has an input connected to a lock signal output of a delay locked loop (DLL) (230), and an output linked to configurable **logic blocks** (CLB) (205). A global clock network (235) has an input connected to the clock output terminal of the DLL, and distributed clock terminals connected to **logic-block** clock terminals to send a clock signal to each configurable **logic block**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for preparing a **programmable logic device** to perform logic function.

USE - For configuring **field programmable gate array** (**FPGA**).

ADVANTAGE - Reduces risk of error due to unstable clock signal. Has **integrated** locked **loop** that produces a lock signal internal to the programmable gate array and maintains lock on the clock signal so that the sequencer will not wait the lock signal after reconfiguration. Allows sequencer to disable the **FPGA** until the lock signal is received.

DESCRIPTION OF DRAWING(S) - The figure is a partially schematic diagram of a **field programmable gate array**.

CLB (205)
DLL (230)
Global clock network (235)
Sequencer (240)
pp; 10 DwgNo 2/5

31/3,AB/27 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013733010
WPI Acc No: 2001-217240/200122
Related WPI Acc No: 1998-271292; 1999-571366; 2001-662213
XRPX Acc No: N01-154736
Programmable logic integrated circuit with clock distribution function, has multiplexer that selectively couples reference or synchronized clock output signal to input of **logic block**
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: CLIFF R G; COPE L T; JEFFERSON D E; REDDY S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 6130552 A 20001010 US 95543420 A 19951016 200122 B
US 97971315 A 19971117
US 98165463 A 19981002

Priority Applications (No Type Date): US 95543420 A 19951016; US 97971315 A 19971117; US 98165463 A 19981002
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6130552	A		23	G06F-007/38	Cont of application US 95543420 Div ex application US 97971315 Cont of patent US 5744991

Abstract (Basic): US 6130552 A
Abstract (Basic):

NOVELTY - Global horizontal and vertical interconnects couple **logic blocks** of an array mutually. A clock synchronization circuit such as delay or phase lock loop generates synchronous clock output signal, by receiving reference and feedback clock signal. A multiplexer selectively couples reference or synchronized clock output signal to input of **logic block**.

USE - In e.g. **programmable logic integrated circuit** device (**PLD**), field **programmable logic** array (**FPGA**) with clock distribution scheme using delay or phase locked **loop** in semiconductor **integrated circuit** fabrication.

ADVANTAGE - Clock synchronous circuit reduces or minimizes clock skew when distributing clock signal within **integrated circuit**, thus **IC** performance is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of delay lock loop using micro and macro phase detector.

pp; 23 DwgNo 4/11

31/3,AB/28 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013661809
WPI Acc No: 2001-146021/200115
XRPX Acc No: N01-106794
Integrated circuit e.g. **field programmable gate array**, has disable circuit which is configured to disable first **logic block** among several **logic blocks**, and is coupled to first **logic block**
Patent Assignee: XILINX INC (XILI-N)
Inventor: BURNHAM J L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6160418	A	20001212	US 99231532	A	19990114	200115	B

Priority Applications (No Type Date): US 99231532 A 19990114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6160418	A		17	H03K-019/177	

Abstract (Basic): US 6160418 A
Abstract (Basic):

NOVELTY - The **integrated circuit** comprises several **logic blocks** and a disable circuit (370). The disable circuit is coupled to first **logic block** among several **logic blocks** and is configured to disable the first **logic block**.

USE - For **field programmable gate array** (**FPGA**), application specific **integrated circuit** (ASIC), microprocessor and **programmable logic device** (**PLD**).

ADVANTAGE - Provides the versatility of multiple product lines by selectively disabling **logic block** within an **integrated circuit**.

DESCRIPTION OF DRAWING(S) - The figure shows the simplified schematic diagram of **FPGA**.

Disable circuit (370)

pp; 17 DwgNo 3/11

31/3,AB/29 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013661747
WPI Acc No: 2001-145959/200115
Related WPI Acc No: 2002-370383
XRPX Acc No: N01-106741

Programmable logic device such as **programmable logic** array includes power supply enable circuit which powers ON or OFF of **logic blocks** when **logic block** are enabled or disabled respectively

Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: LACEY T M; MACARTHUR J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6148390	A	20001114	US 96662054	A	19960612	200115 B

Priority Applications (No Type Date): US 96662054 A 19960612
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6148390	A		11	G06F-001/26	

Abstract (Basic): US 6148390 A
Abstract (Basic):

NOVELTY - One set of **logic blocks** in several sets of **logic blocks** (310a-310n) consists of several **logic blocks** and a power supply enable circuit having inputs to receive source voltage, ground voltage via **logic blocks** and enable bit respectively. The power supply enable circuit powers ON or OFF the **logic blocks**, when the **logic blocks** are enabled or disabled respectively.

DETAILED DESCRIPTION - Several routing resources (320a-320n) corresponding to enabled **logic blocks** provide data paths for the enabled **logic blocks** and routing resources corresponding to disabled **logic blocks** bypass the disabled **logic blocks**. A programming circuit (370) stores configuration data which are provided to routing resources corresponding to the enabled **logic blocks**. An INDEPENDENT

CLAIM is also included for programming method of **programmable logic device**.

USE - **Programmable logic device** e.g. application specific **integrated circuit** such as **programmable** array **logic**, **programmable logic** array, field **programmable logic** array, **field programmable gate array**, electrically erasable **programmable logic device**, liquid crystal array.

ADVANTAGE - Provides redundant **logic blocks** utilized by programming software, to reduce the probability of producing defective **programmable logic devices**. Provides **programmable logic device** that has the software capability to program around a bad or non-functional **logic block**.

DESCRIPTION OF DRAWING(S) - The figure shows the illustration of routing configuration bypass circuit.

Logic blocks (301a-301n)
Routing resources (320a-320n)
Programming circuit (370)
pp; 11 DwgNo 3/5

31/3,AB/30 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013051197
WPI Acc No: 2000-223051/200019
Related WPI Acc No: 1998-520629
XRPX Acc No: N00-167101

Field programmable gate array chip for **programmable logic device** used in computer, has two control circuits that operate configurable function **block** as **programmable logic** and **block** of memory, respectively

Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: CHINNOW D H; STEELE R C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6029236	A	20000222	US 97790271	A	19970127	200019 B
			US 97972656	A	19971118	

Priority Applications (No Type Date): US 97790271 A 19970127; US 97972656 A 19971118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6029236	A		27	G06F-012/00	Cont of application US 97790271 Cont of patent US 5809281

Abstract (Basic): US 6029236 A
Abstract (Basic):

NOVELTY - Two control circuits are configured to operate configurable function **block** (CFB) as **programmable logic** and **block** of memory, respectively. The CFB performs predetermined logic operation on input signals, when configured as **programmable logic**. Read/write circuit of one control circuit read or write data from or to the preconfigured SRAM cells in another control circuit.

DETAILED DESCRIPTION - One control circuit comprises non-volatile architectural elements connected to several preconfigured SRAM cells that are connected to AND and OR logical gate arrays. Another control circuit comprises read/write circuit. INDEPENDENT CLAIMS are also included for the following:

(a) method of operating configurable function block;

(b) switching cell

USE - For **programmable logic device** used in computer system.

ADVANTAGE - When CFB is configured as either high performance **programmable logic** or **block** of SRAM, user can initially program the desired equation into non-volatile cells in non-volatile architectural element or SRAM cells in volatile logic array are utilized to store data, rather than determining programmable connections, thus effective programming is realizable.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of **field programmable gate array**.

pp; 27 DwgNo 1/15

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34/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6971101 INSPEC Abstract Number: B2001-08-1265B-042, C2001-08-5210B-063
Title: High-quality **FPGA** designs through functional decomposition with sub-function input support selection based on information relationship measures
Author(s): Chojnacki, A.; Jiwiak, L.
Author Affiliation: Eindhoven Univ. of Technol., Netherlands
Conference Title: Proceedings of the IEEE 2001. 2nd International Symposium on Quality Electronic Design p.409-14
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2001 Country of Publication: USA xxi+497 pp.
ISBN: 0 7695 1025 6 Material Identity Number: XX-2001-00569
U.S. Copyright Clearance Center Code: 0 7695 1025 6/2001/$10.00
Conference Title: Proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design. IEEE ISQED 2001
Conference Sponsor: IEEE Tech. Committee on VLSI Design (TCVLSI); IEEE Comput. Soc. Tech. Committee on Design Autom. (TCDA); IEEE Comput. Soc. Test Technol. Tech. Council (TTTC)
Conference Date: 26-28 March 2001 Conference Location: San Jose, CA, USA
Language: English
Abstract: Functional decomposition seems to be the most effective circuit synthesis approach for look-up table (LUT) FPGAs, (C)**PLDs** and complex gates. Since LUT FPGAs are used in numerous important applications and constitute a foundation for the novel re-configurable system-on-a-**chip** platforms, an adequate synthesis for this target is of primary importance for the modern system industry. In the functional decomposition targeting LUT FPGAs, the circuit is constructed by recursively decomposing a given function and its sub-functions until each of the resulting sub-functions can be directly implemented with a LUT. The impact support selection for the sub-functions that are constructed in this process decides the quality of the resulting multi-level circuit to a high degree. In this paper; we propose a new effective method for the sub-function input support selection and discuss its application in our circuit synthesis tool that targets LUT-based FPGAs. The experimental results demonstrate that the proposed approach lends to extremely fast and very small circuits. The circuits consume on average over 2 times less **logic blocks** (CLBs) and are over 1.5 times faster than the circuits produced by the best state-of-the-art commercial tools.
Subfile: B C

34/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6964636 INSPEC Abstract Number: B2001-08-1265B-024, C2001-08-5210B-026
Title: High-quality sub-function construction in functional decomposition based on information relationship measures
Author(s): Jozwiak, L.; Chojnacki, A.
Author Affiliation: Eindhoven Univ. of Technol., Netherlands
Conference Title: Proceedings Design, Automation and Test in Europe. Conference and Exhibition 2001 p.383-90

Editor(s): Nebel, W.; Jerraya, A.
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2001 Country of Publication: USA xxxvi+829 pp.
ISBN: 0 7695 0993 2 Material Identity Number: XX-2001-00575
U.S. Copyright Clearance Center Code: 1530-1591/2001/$10.00
Conference Title: Proceedings Design, Automation and Test in Europe. Conference and Exhibition 2001
Conference Sponsor: EDAA; EDAC; IEEE-CS TTTC; IEEE-CS DATC; ECSI; RAS Russian Acad. Sci.; IPPM; ACM-SIGDA; IFIP 10.5; AEIA; ATI; CLRC; CNR; Estonian E Soc.; GI; GMM; HTE; ITG; KVIV; VDE
Conference Date: 13-16 March 2001 Conference Location: Munich, Germany
Language: English
Abstract: Functional decomposition seems to be the most effective circuit synthesis approach for look-up table (LUT) FPGAs, (C)**PLDs** and complex gates. In the functional decomposition that targets LUT FPGAs, the circuit is constructed by recursively decomposing a given function and its sub-functions until each of the resulting sub-functions can be directly implemented with a LUT. The choice of sub-functions constructed in this process decides the quality of the resulting multi-level circuit expressed in terms of the **logic block** count and speed. In this paper, we propose a new effective and efficient method for the sub-function construction, and we consider its application in our circuit synthesis tool that targets LUT-based FPGAs. The method is based on the information relationship measures. The experimental results demonstrate that the proposed approach leads to extremely fast and very small circuits.
Subfile: B C

34/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

4654676 INSPEC Abstract Number: B9406-1265B-029, C9406-5120-006
Title: Use LFSRs to build fast **FPGA**-based counters
Author(s): Klein, B.
Author Affiliation: AT&T Bell Labs., Columbia, MD, USA
Journal: Electronic Design vol.42, no.6 p.87-8, 90, 94, 96-7
Publication Date: 21 March 1994 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
U.S. Copyright Clearance Center Code: 0013-4872/94/$1.00+.50
Language: English
Abstract: The design of larger, faster synchronous counters based on either complex **PLDs** (CPLDs) or field-programmable gate arrays (FPGAs) is fraught with speed and density trade-offs. The engineer's best avenue is dedicated circuitry for counters that doesn't consume routing resources external to the basic logic element. The size of the logic element needs to balance the conflicting goals of flexibility (best implemented with small or fine-grain **logic blocks**) and functionality (best implemented with large or course-grain **logic blocks**). That's what third-generation SRAM-based FPGAs provide through a multigrain, configurable lookup-table (LUT) architecture. This architectural feature coupled with a counter-design technique called maximal-length linear feedback shift registers (LFSRs) overcomes fast counter design limitations. Such an **FPGA** -based design can yield counter speeds of 100 MHz and beyond without consuming inordinate logic and routing resources.
Subfile: B C

34/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4502584 INSPEC Abstract Number: B9311-1265B-121, C9311-5120-026
Title: Architecture of field-programmable gate arrays
Author(s): Rose, J.; El Gamal, A.; Sangiovanni-Vincentelli, A.
Author Affiliation: Dept. of Electr. Eng., Toronto Univ., Ont., Canada
Journal: Proceedings of the IEEE vol.81, no.7 p.1013-29
Publication Date: July 1993 Country of Publication: USA
CODEN: IEEPAD ISSN: 0018-9219
U.S. Copyright Clearance Center Code: 0018-9219/93/$03.00
Language: English
Abstract: A survey of **field-programmable gate array** (**FPGA**) architectures and the programming technologies used to customize them is presented. Programming technologies are compared on the basis of their volatility, size parasitic capacitance, resistance, and process technology complexity. **FPGA** architectures are divided into two constituents: **logic block** architectures and routing architectures. A classification of **logic blocks** based on their granularity is proposed, and several **logic blocks** used in commercially available FPGAs are described. A brief review of recent results on the effect of **logic block** granularity on **logic** density and performance of an **FPGA** is then presented. Several commercial routing architectures are described in the context of a general routing architecture model. Finally, recent results on the tradeoff between the flexibility of an **FPGA** routing architecture, its routability, and its density are reviewed.
Subfile: B C

34/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04267612 INSPEC Abstract Number: C9212-5120-007
Title: Automatic circuit partitioning in the Anyboard rapid prototyping system
Author(s): Thomae, D.A.; Van den Bout, D.E.
Author Affiliation: Dept. of Electr. & Comput. Eng., North Carolina State Univ., Raleigh, NC, USA
Journal: Microprocessors and Microsystems vol.16, no.6 p.283-90
Publication Date: 1992 Country of Publication: UK
CODEN: MIMID5 ISSN: 0141-9331
U.S. Copyright Clearance Center Code: 0141-9331/92/060283-08$3.00
Language: English
Abstract: The Anyboard rapid prototyping system is described. The Anyboard circuit partitioner is discussed and the results of experiments are presented that characterize its ability to find good partitions. Under some conditions it was found that an algorithm that is generally regarded as poor in fact produces good results in less time than an algorithm that is generally regarded as more powerful. The standard Anyboard PC card holds five **FPGA**, which may be any of the 3000 series Xilinx **FPGA**, (field programmable gate arrays), although the Anyboard software can handle any number of **FPGA** in any configuration. The partitioner determines which **logic blocks** go on which **chips**, taking into account the effects of partitioning on clock rate, the I/O requirements of the

design and the limit on the amount of logic that each **FPGA** can contain.
Subfile: C

34/3,AB/6 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08420236 Genuine Article#: 284BJ Number of References: 8
Title: An approach for detecting multiple faulty **FPGA logic blocks** (ABSTRACT AVAILABLE)
Author(s): Huang WK (REPRINT) ; Meyer FJ; Lombardi F
Corporate Source: FUDAN UNIV,ASIC & SYST STATE KEY LAB/SHANGHAI 200433//PEOPLES R CHINA/ (REPRINT); NORTHEASTERN UNIV,DEPT ELECT & COMP ENGN/BOSTON//MA/02115
Journal: IEEE TRANSACTIONS ON COMPUTERS, 2000, V49, N1 (JAN), P48-54
ISSN: 0018-9340 Publication date: 20000100
Publisher: IEEE COMPUTER SOC, 10662 LOS VAQUEROS CIRCLE, PO BOX 3014, LOS ALAMITOS, CA 90720-1314
Language: English Document Type: ARTICLE
Abstract: An approach is proposed to test **FPGA logic blocks**, including part of the configuration memories used to control them. The proposed AND tree and OR tree-based testing structure is simple and the conditions for constant testability can easily be satisfied. Test generation for only a single **logic block** is sufficient. We do not assume any particular fault model. Any number of faulty blocks in the **chip** can be detected. Members of the Xilinx XC3000, XC4000, and XC5200 families were studied. The proposed AND/OR approach was found to reduce the number of **FPGA** reprogrammings needed for testing;by up to a factor of seven versus direct methods of multiple faulty block detection.

34/3,AB/7 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04820992 JICST ACCESSION NUMBER: 01A0224810 FILE SEGMENT: JICST-E
LUT Granularity Evaluation for Reconfigurable Logic.
IIDA MASAHIRO (1); SUEYOSHI TOSHINORI (2)
(1) Kumamotodai Daigakuinshizenkagakukenkyuka; (2) Kumamoto Univ., Fac. of Eng.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2000, VOL.100,NO.475(FTS2000 34-75), PAGE.77-82, FIG.7, TBL.6, REF.13
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.37:681.325.6 621.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: There are some problems in present **FPGA** that a reconfiguration takes time. These are the cause that performance with the reconfigurable computing can't be drawn. In this paper, We cleared the necessary condition of the programable logic which is suitable for the reconfigurable computing and evaluated about the granularity of LUT on three measures of the implementation area, the critical path delay

and the implementation efficiency. As a result, it was found out that the LUT granularity that it got a minimum area became large when fixed field in the **logic block** increase. Moreover, as for the critical path delay, the best LUT granularity varied in the circuit, and 5-LUT showed minimum delay on the average of the evaluation circuit. Then, implementaion efficiency was decrease in according to LUT granularity's becoming large, and it was found out that it was less than 50% in 7-LUT. (author abst.)

34/3,AB/8 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02538225 JICST ACCESSION NUMBER: 95A0617275 FILE SEGMENT: JICST-E
A Hierarchical Circuit Partitioning Algorithm for Multi-**FPGA** Systems.
TOGAWA NOZOMU (1); SATO MASAO (1); OTSUKI TATSUO (1)
(1) Waseda Univ., Sch. of Sci. & Eng.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.112(DSP95 63-77), PAGE.69-76, FIG.8, TBL.6, REF.15
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In this paper, we propose an algorithm which partitions an initial circuit into multi-**FPGA chips**. The algorithm is based on recursive bi-partitioning of a circuit. In each bi-partitioning, it searches a partitioning position of a circuit such that each of partitioned subcircuits is accommodated in each **FPGA chip** with making the number of signal nets between **chips** as small as possible. Such bi-partitioning is achieved by computing a minimum cut repeatedly applying a network flow technique, and replicating **logic-blocks** appropriately. Since a set of **logic-blocks** assigned to each **chip** is computed separately, **logic-blocks** to be replicated are naturally determined. This means that the algorithm makes good use of unused **logic-blocks** from the viewpoint of reducing the number of signal nets between **chips**, i.e. the number of required I/O blocks. Experimental results for several benchmark circuits show its efficiency and effectiveness. (author abst.)

34/3,AB/9 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02233356 JICST ACCESSION NUMBER: 94A0866990 FILE SEGMENT: JICST-E
Maple: A Simultaneous Technology Mapping, Placement, and Global Routing Algorithm for LUT-based FPGAs.
SATO MASAO (1); TOGAWA NOZOMU (1); OTSUKI TATSUO (1)
(1) Waseda Univ., Sch. of Sci. & Eng.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1994, VOL.94,NO.257(CPSY94 55-60), PAGE.41-48, FIG.10, TBL.6, REF.19
JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 681.325/.326.009.18
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Technology mapping algorithms for LUT(Look Up Table) based FPGAs have aimed at transforming a Booleau network into **logic-blocks**. However, since those algorithms take no layout information into account, they cannot produce excellent layout results. In this paper, a simultaneous technology mapping, placement and global routing algorithm for FPGAs, Maple, is presented. Maple is an extended version of a simultaneous placement, and global routing algorithm for FPGAs, which is based on recursive partition of layout regions and block sets. Maple inherits its basic process and executes the technology mapping simultaneously in each recursive process. Therefore, the mapping can be done with the placement and global routing information. Experimental results for some benchmark circuits demonstrate its efficiency and effectiveness. (author abst.)

34/3,AB/10 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02039046 JICST ACCESSION NUMBER: 94A0340049 FILE SEGMENT: JICST-E
Design technique of **FPGA/PLD**.Design technique which utilizes a characteristic of **FPGA** in video signal processor. Application examples of Xilinx and Quick Logic.
HIROSHIMA TAMOTSU (1)
(1) Kosumorisachi
Denshi Zairyo(Electronic Parts and Materials), 1994, VOL.33,NO.4, PAGE.100-105, FIG.6, TBL.1
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.37:681.325.6
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Referring to video signal processors based on two kinds of **FPGA** devices, logic cell array and pASIC, features of each **FPGA** and design methods of each one utilizing each character were explained. XC3090 of Xilinx Co., for LCA and QL12*16 of Quick Logic Co. for pASIC were used. Architectures such as a **logic block** constitution and wiring resource in these two kinds of **FPGA**, were compared.

34/3,AB/11 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01899612 JICST ACCESSION NUMBER: 93A0843785 FILE SEGMENT: JICST-E
Special Issue on Synthesis and Verification of Hardware Design. Analysis of the Trends in Logic Synthesis.
SAUCIER G (1)
(1) Inst. National Polytechnique de Grenoble/CSI, Grenoble, FRA
IEICE Trans Inf Syst(Inst Electron Inf Commun Eng), 1993, VOL.E76-D,NO.9, PAGE.1006-1017, FIG.14, TBL.10, REF.16

JOURNAL NUMBER: L1371AAJ ISSN NO: 0916-8532
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper tends to analyze the trends of the research in logic synthesis. The first part is devoted to an expertise of the efficiency of factorization methods developed during the last decade and to the proposal of dedicated methods for complex **logic blocks**. The second part shows the importance of Binary Decision Diagrams as representation of Boolean functions. Their use in the technology mapping phase of multiplexor based FPGAs in an industrial tool is taken as illustration. (author abst.)

34/3,AB/12 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014884385
WPI Acc No: 2002-705091/200276
Related WPI Acc No: 2001-217813; 2001-519802; 2002-253514; 2003-287525
XRPX Acc No: N02-555733
Programmable **integrated circuit** for use in switch, has logic element whose input terminal is selectively coupled to pass input signal through logic function or by passing **logic** functional **block**
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: HEILE F B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6414514	B1	20020702	US 9614942	P	19960405	200276 B
			US 9615122	P	19960410	
			US 97838398	A	19970403	
			US 983415	A	19980105	
			US 2000618317	A	20000718	

Priority Applications (No Type Date): US 2000618317 A 20000718; US 9614942 P 19960405; US 9615122 P 19960410; US 97838398 A 19970403; US 983415 A 19980105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6414514	B1		16	H03K-019/177	Provisional application US 9614942 Provisional application US 9615122 Cont of application US 97838398 Div ex application US 983415

Abstract (Basic): US 6414514 B1
Abstract (Basic):
NOVELTY - The input terminal of a logic element (240) is selectively coupled to pass an input signal through the **logic** function **block**. The input terminal is selectively coupled to pass the input signal unstored to the output terminal by passing the **logic** function **block**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for system including programmable **integrated circuit**.
USE - Programmable **integrated circuit** such as PAL, PLA,

FPLA, **PLD**, CPLD, EPLD, EEPLD, LCA, **FPGA** used in telecommunication system, switch, network, vehicle system, control system, consumer electronics personal computer etc.

ADVANTAGE - The signal on the input terminal can pass through the logic element without having logically altered or stored.

DESCRIPTION OF DRAWING(S) - The figure shows a circuit diagram of the logic element used in larger **logic** array **blocks**.

Logic element (240)

pp; 16 DwgNo 3B/8

34/3,AB/13 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011981695
WPI Acc No: 1998-398605/199834
XRPX Acc No: N98-310162

Field programmable gate array - with hierarchical configuration and state storage using a superset of reconfiguration modes stored in multiple configurations on-**chip**

Patent Assignee: XILINX INC (XILI-N)
Inventor: CARBERRY R A; JOHNSON R A; TRIMBERGER S M; WONG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5778439	A	19980707	US 95517019	A	19950818	199834	B

Priority Applications (No Type Date): US 95517019 A 19950818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5778439	A		85	G06F-012/02	

Abstract (Basic): US 5778439 A

The device comprises an active memory containing configurable **logic blocks** (1100), inactive memory (1102) containing inactive configuration, which can be provided partially or entirely off-**chip**, sequential logic (110) and routing provided by the active configuration; connected by data (Dbus) and address (Abus) buses. Memory address register MAR (1105), memory data register MDR (1103) and column data register CDR (1108) are provided. The width of the MDR is programmable, with typical values of 1,2 or 4 bytes. The width of the CDR is that of the data bus, allowing multiple transfers of MDR for every transfer of CDR.

On-**chip** timing and address decoding (1107), together with memory controller (1106), control configuration of **logic blocks** and routing.

ADVANTAGE - Reconfiguration is simply achievable due to on-**chip** storage of configurations.

Dwg.11/64

34/3,AB/14 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010528564
WPI Acc No: 1996-025517/199603

XRPX Acc No: N96-021652
High speed **FPGA** - uses **FPGA logic block** which is programmed by using SRAM in which rewriting or changing of data is possible
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7297291	A	19951110	JP 9489025	A	19940427	199603	B

Priority Applications (No Type Date): JP 9489025 A 19940427
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7297291	A		5	H01L-021/82	

Abstract (Basic): JP 7297291 A

The array uses a comparatively small scale **PLD** block (7) of one-time-write type structure which is programmed by using an anti-fuse to control the delay time of a wiring route.

A large scale **FPGA** block (8) is connected to the **PLD** block and both blocks are connected to a logic signal input and output port (9) via internal wiring (11). The **FPGA** block is connected to a SRAM block in which rewriting is possible, via external wiring (12).

ADVANTAGE - Enables high speed logic **circuit** large scale **integration** in just one **chip**.

Dwg.1/8

34/3,AB/15 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010377578
WPI Acc No: 1995-278892/199537
XRPX Acc No: N95-212852
Circuit with user request logic circuit programme in design spot such as **PLD**, **FPGA** - has **logic block** with by-pass wiring, with I-O buffer circuit which sends and receives data between **chip** exterior and any circuit contg. **logic block** in **chip**
NoAbstract
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7176616	A	19950714	JP 93317877	A	19931217	199537	B

Priority Applications (No Type Date): JP 93317877 A 19931217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7176616	A		5	H01L-021/82	

34/3,AB/16 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05004691
FIELD PROGRAMMABLE GATE ARRAY

PUB. NO.: 07-297291 [JP 7297291 A]
PUBLISHED: November 10, 1995 (19951110)
INVENTOR(s): HATA EIZO
AOYAMA KAZUAKI
NAKAMURA HIROYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-089025 [JP 9489025]
FILED: April 27, 1994 (19940427)

ABSTRACT

PURPOSE: To achieve a large-scale logic including a high-speed circuit with a single **chip**.

CONSTITUTION: A relatively small-scale first **logic block** 7 (**PLD**) in a write once structure where programming is performed using an anti-fuse and a large- scale second **logic block** 8 (**FPGA**) where programming can be performed repeatedly using a memory element 10 such as SRAM are mutually connected via an internal wiring 11 and at the same time I/O of a logic signal etc., is performed with the outside via an external I/O board 9 in a one-**chip field programmable gate array** 6.

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  08sep03 13:00:57 User267149 Session D971.1

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  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200357
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/May(Updated 030902)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	95	AU=(GAN, A? OR GAN A?)
S2	1	S1 AND ((INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?)
S3	94	S1 NOT S2
S4	0	S3 AND PROGRAMMAB??????(3N)LOGIC
S5	0	S3 AND ((HORIZONTAL?????? OR VERTICAL????? OR DISSIMILAR??-?? OR DIFFERENT????? OR VARIOUS???? OR COMPROMIS????? OR ONE - OR FIRST OR TWO OR SECOND)(3N)PITCH??????)

2/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403861
WPI Acc No: 2002-224564/200228
XRPX Acc No: N02-172029
Computer-readable medium for designing ASIC, stores data structure with data fields representing power conductors extending through cell area of ASIC
Patent Assignee: XILINX INC (XILI-N)
Inventor: BAXTER G A; **GAN A H**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6308309	B1	20011023	US 99374254	A	19990813	200228	B

Priority Applications (No Type Date): US 99374254 A 19990813
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6308309	B1		12	G06F-019/00	

Abstract (Basic): US 6308309 B1
Abstract (Basic):
NOVELTY - The medium stores data structure with data fields containing respective data representing power conductors extending through a cell area (500) of an ASIC to be designed. Another data field contains data representing a signal conductor (535) extending between input and output ports. The signal conductor is electrically isolated from active components within the cell area.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Stopper cell in ASIC;
(b) **Integrated circuit;**
(c) Method of routing functional blocks of **integrated circuit**
USE - For use in designing application specific **integrated circuit** (ASIC) including field programmable gate array (FPGA) and programmable logic devices.
ADVANTAGE - Provides recording medium that enables designing custom blocks of FPGA in parallel with the placement and routing of the blocks, thus reducing time to market for ASIC.
DESCRIPTION OF DRAWING(S) - The figures show the flowchart depicting the design flow for ASIC, and exemplary view of oxide-isolated gate array stopper cell.
Cell area of ASIC (500)
Signal conductor (535)
pp; 12 DwgNo 3, 5A/6